International
IOR Rectifier

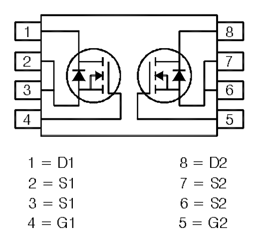
PD - 96246

IRF8852PbF

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Dual N-Channel MOSFET
- Very Small SOIC Package
- Low Profile (< 1.1mm)
- Available in Tape & Reel
- Lead-Free

V_{DSS}	$R_{DS(on)}$ max	Id
25V	11.3mΩ@V_{GS} = 10V	7.8A
	15.4mΩ@V_{GS} = 4.5V	6.2A



TSSOP-8

Description

HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design, that International Rectifier is well known for, provides the designer with an extremely efficient and reliable device for battery and load management.

The TSSOP-8 package has 45% less footprint area than the standard SO-8. This makes the TSSOP-8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.2mm) allows it to fit easily into extremely thin environments such as portable electronics and PCMCIA cards.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	25	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	7.8	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	6.2	
I_{DM}	Pulsed Drain Current ①	62.4	
P_D @T_A = 25°C	Power Dissipation ④	1.0	W
P_D @T_A = 70°C	Power Dissipation ④	0.64	
	Linear Derating Factor	0.01	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	——	53	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④	——	125	

Notes ① through ⑤ are on page 10

ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.

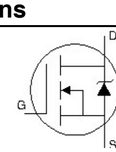
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.02	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	9.2	11.3	mΩ	V_{GS} = 10V, I_D = 7.8A ③
		—	12.5	15.4		V_{GS} = 4.5V, I_D = 6.2A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.8	2.35	V	V_{DS} = V_{GS}, I_D = 25μA
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	V_{DS} = 20V, V_{GS} = 0V
		—	—	150		V_{DS} = 20V, V_{GS} = 0V, T_J = 70°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	19	—	—	S	V_{DS} = 10V, I_D = 7.8A
Q_g	Total Gate Charge	—	9.5	—	nC	I_D = 7.8A,V_{DS}= 13V, V_{GS} = 4.5V
Q_g	Total Gate Charge	—	17.4	26.1	nC	I_D = 7.8A
Q_{gs}	Gate-to-Source Charge	—	3.1	—		V_{DS} = 13V
Q_{gd}	Gate-to-Drain Charge	—	2.9	—		V_{GS} = 10V
R_G	Gate Resistance	—	2.8	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	11.4	—	ns	V_{DD} = 13V, V_{GS} = 10V ③
t_r	Rise Time	—	10.9	—		I_D = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	—	70.8	—		R_D =13 Ω
t_f	Fall Time	—	28.9	—		R_G =30 Ω
C_{iss}	Input Capacitance	—	1151	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	295	—		V_{DS} = 20V
C_{rss}	Reverse Transfer Capacitance	—	134	—		ƒ = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	6.5	mJ
I_{AR}	Avalanche Current ①	—	7.8	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.3	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	62.4		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 1.3A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	32	48	ns	T_J = 25°C, I_F = 1.3A, V_{DD} = 20V
Q_{rr}	Reverse Recovery Charge	—	17	26	nC	di/dt = 100A/μs ③

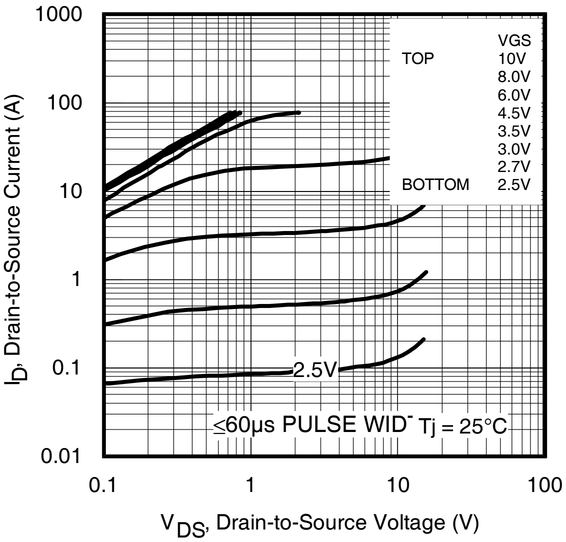


Fig 1. Typical Output Characteristics

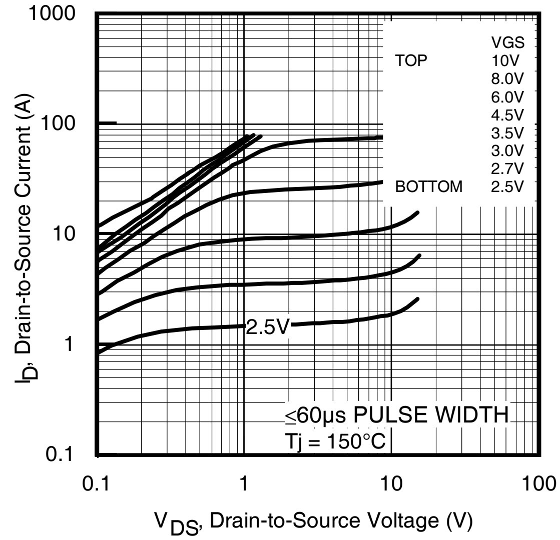


Fig 2. Typical Output Characteristics

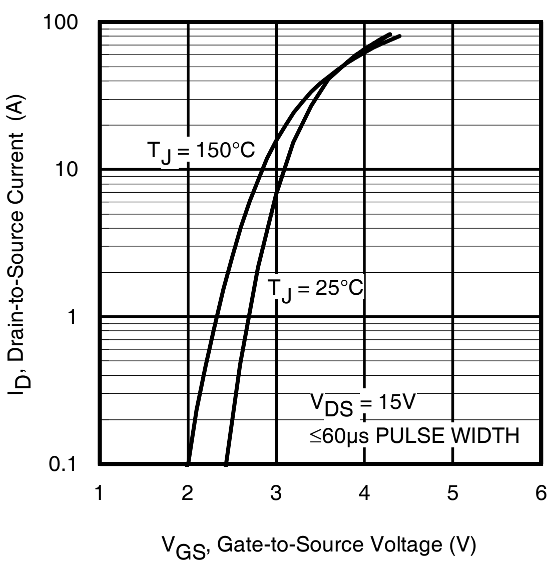


Fig 3. Typical Transfer Characteristics

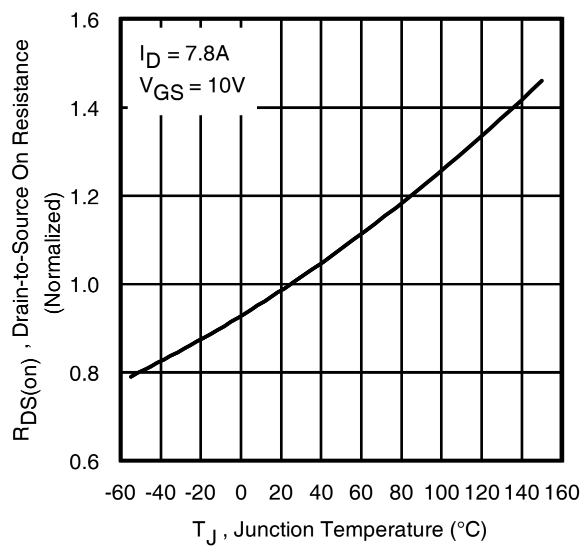


Fig 4. Normalized On-Resistance vs. Temperature

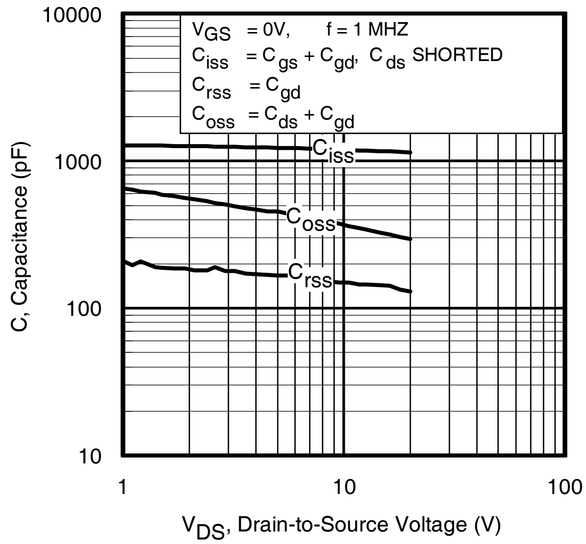


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

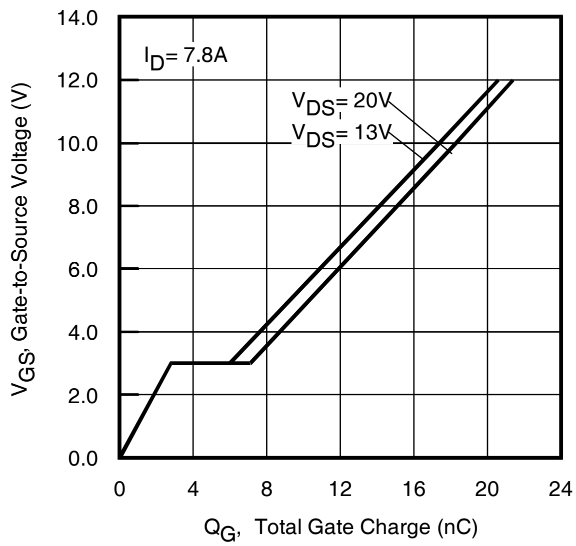


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

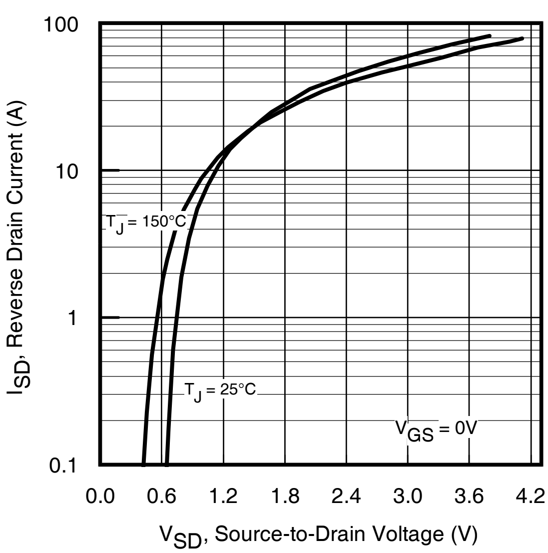


Fig 7. Typical Source-Drain Diode Forward Voltage

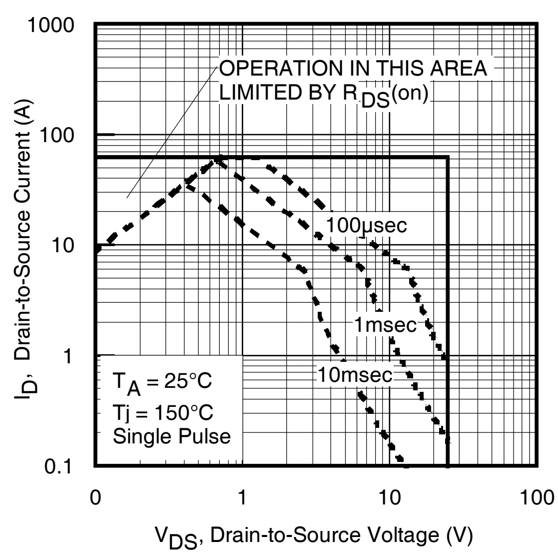


Fig 8. Maximum Safe Operating Area

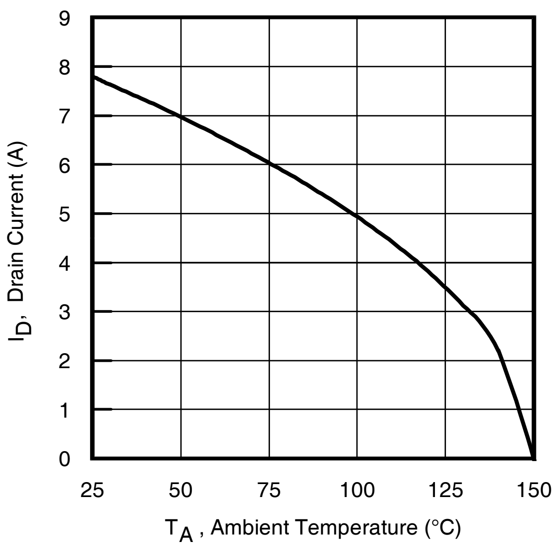


Fig 9. Maximum Drain Current vs. Ambient Temperature

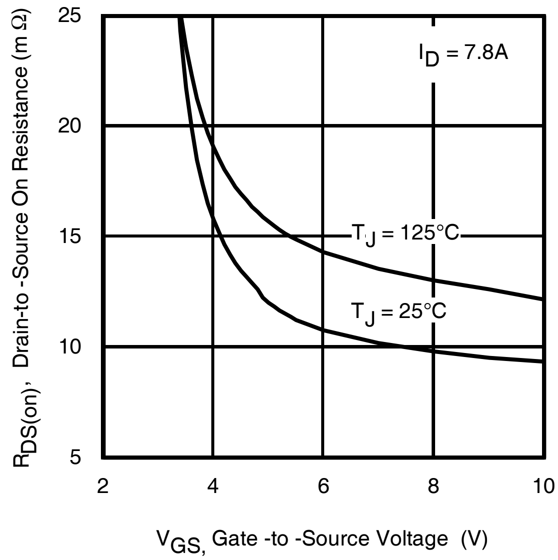


Fig 10. Typical On-Resistance Vs. Gate Voltage

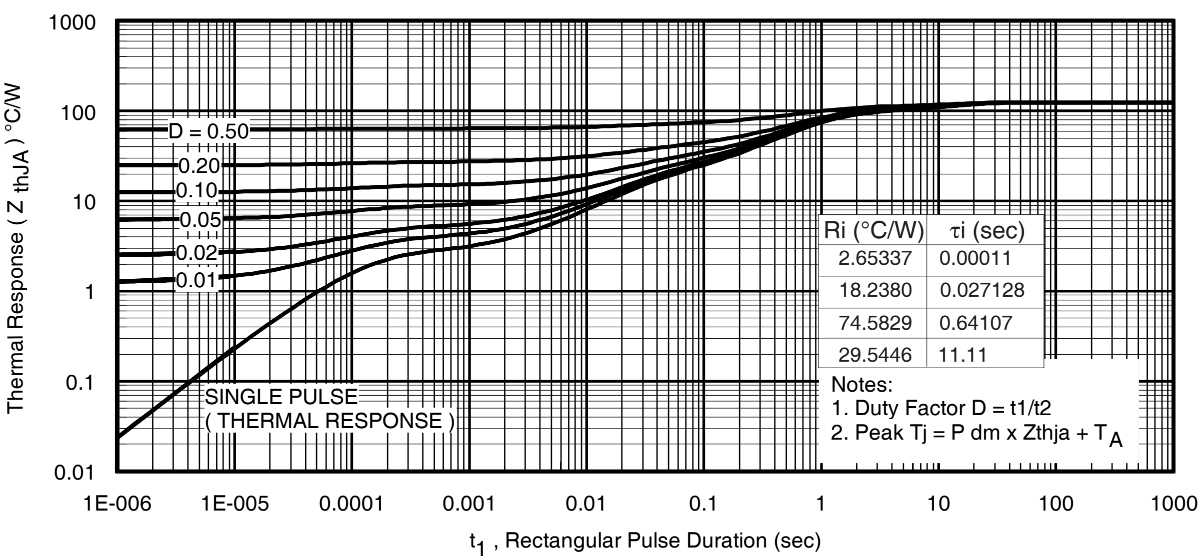


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

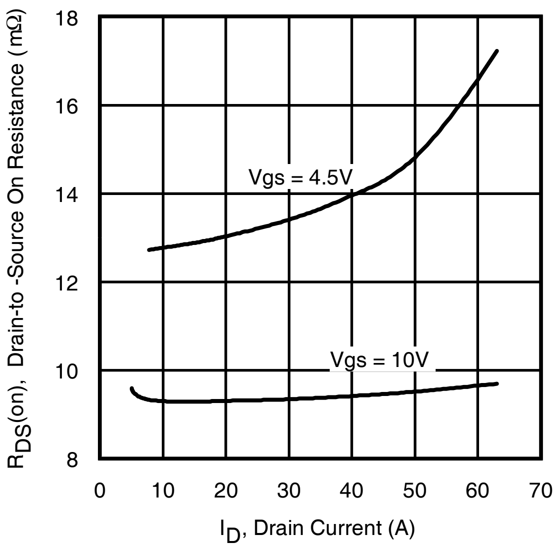


Fig 12. Typical On-Resistance vs. Drain Current

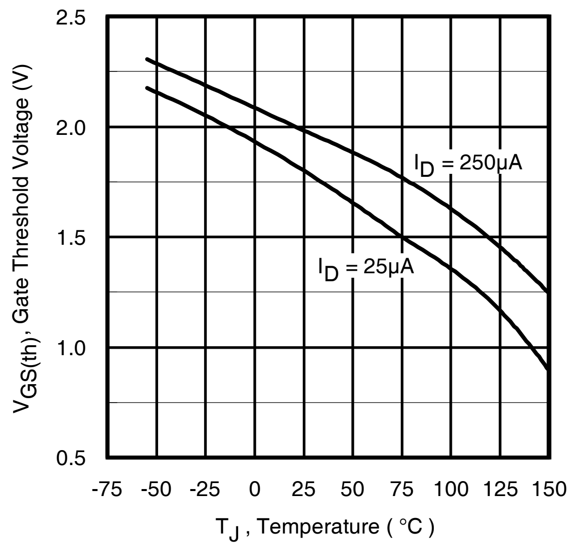


Fig 13. Typical Threshold Voltage vs. Junction Temperature

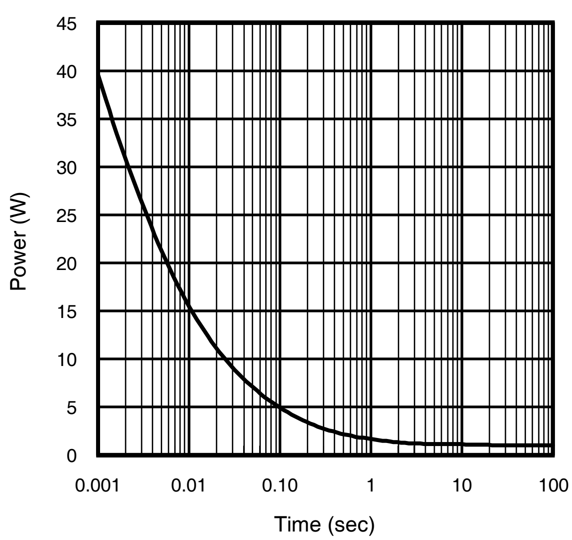


Fig 14. Typical Power Vs. Time

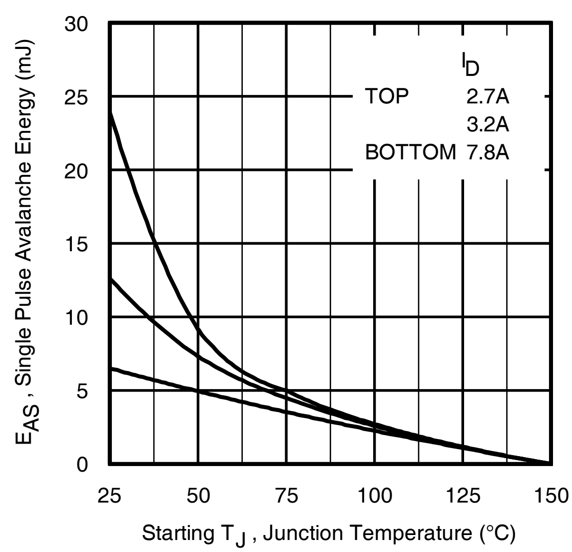


Fig 15. Maximum Avalanche Energy vs. Drain Current

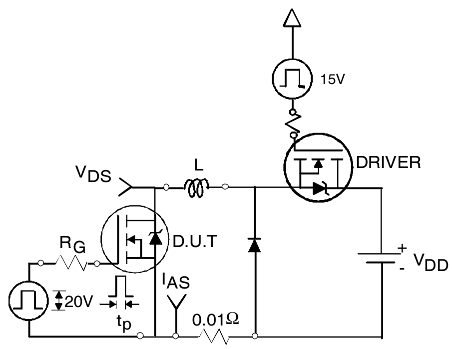


Fig 16a. Unclamped Inductive Test Circuit

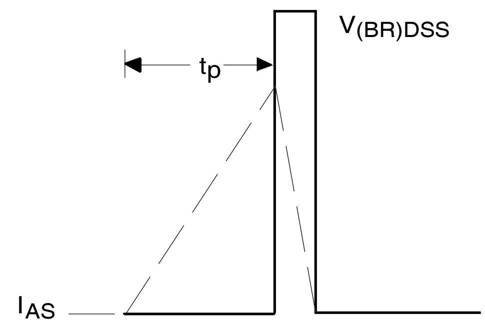


Fig 16b. Unclamped Inductive Waveforms

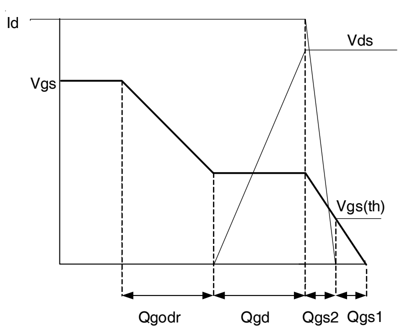


Fig 17. Gate Charge Waveform

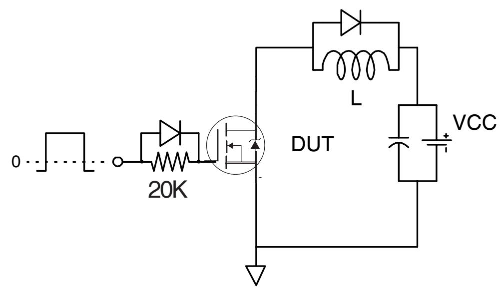


Fig 17. Gate Charge Test Circuit

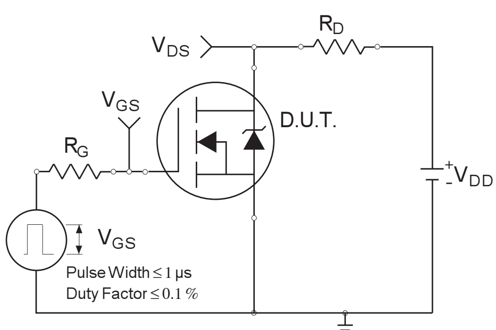


Fig 18a. Switching Time Test Circuit

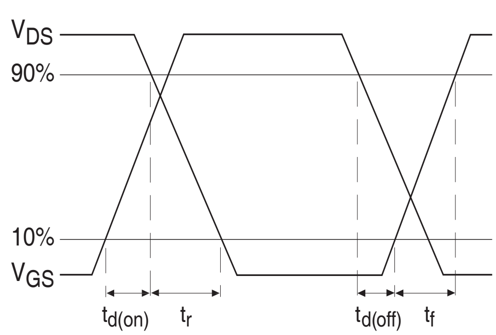
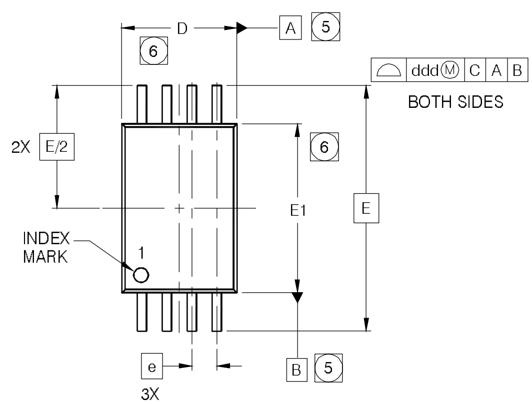


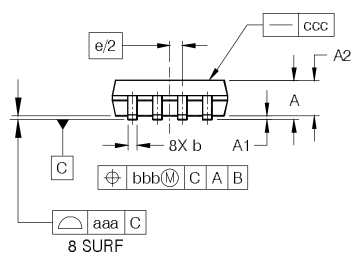
Fig 18b. Switching Time Waveforms

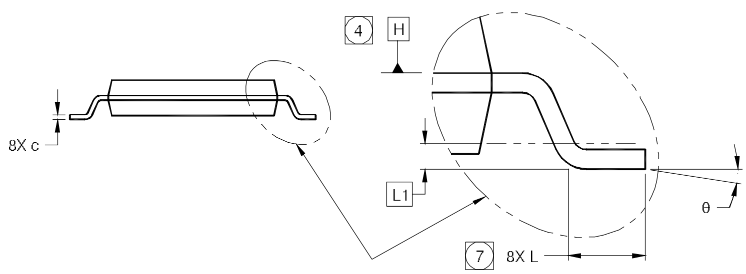
TSSOP8 Package Outline

Dimensions are shown in milimeters (inches)

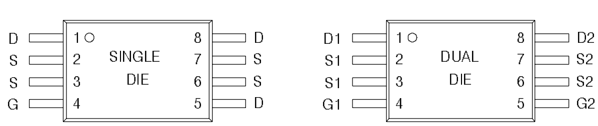


SYMBOL	MO-153AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	.0472
A1	0.05	---	0.15	.0020	---	.0059
A2	0.80	1.00	1.05	.032	.039	.041
b	0.19	---	0.30	.0075	---	.0118
c	0.09	---	0.20	.0036	---	.0078
D	2.90	3.00	3.10	.115	.118	.122
E	6.40 BSC			.251 BSC		
E1	4.30	4.40	4.50	.170	.173	.177
e	0.65 BSC			.0256		
L	0.45	0.60	0.75	.0178	.0236	.0290
L1	0.25 BSC			.010 BSC		
θ	0°	---	8°	0°	---	8°
aaa	0.10			.0039		
bbb	0.10			.0039		
ccc	0.05			.0019		
ddd	0.20			.0078		





LEAD ASSIGNMENTS

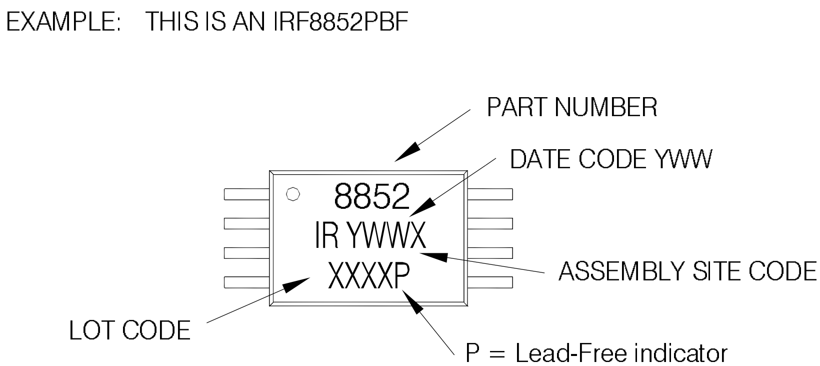


NOTES

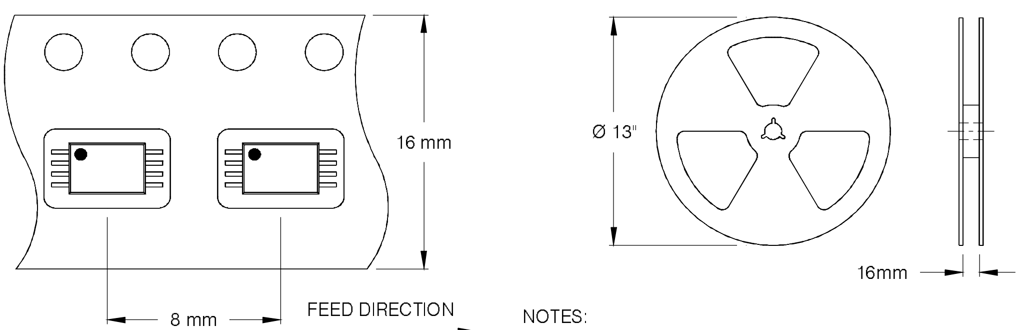
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AS SHOWN.
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE M0-153AA.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

TSSOP8 Part Marking Information



TSSOP-8 Tape and Reel Information



NOTES:
1. TAPE & REEL OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRF8852TRPbF	TSSOP-8	Tape and Reel	4000	

Qualification Information†

Qualification level	Consumer ††	
	(per JEDEC JESD47F††† guidelines)	
Moisture Sensitivity Level	TSSOP-8	MSL1 (per JEDEC J-STD-020D†††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://ww.irf.com

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting T_J = 25°C, L = 0.214mH, R_G = 25Ω, I_{AS} = 7.8A.
③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
④ When mounted on 1 inch square copper board.
⑤ R_θ is measured at T_J of approximately 90°C.

Data and specifications subject to change without notice.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
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