International
IOR Rectifier

IRS21952SPBF

HIGH SIDE & DUAL LOW SIDE DRIVER IC

Features

- 2 low side output channels sharing common ground
- 1 high side output channel
- CMOS Schmitt trigger inputs with pull down resistor
- Under voltage lockout on all channels
- 5 V compatible logic level Inputs
- Immune to –Vs spike and tolerant to dVs/dt & dVss/dt
- Shoot through prevention logic

Descriptions

The IRS21952 contains 2 low side outputs sharing common ground and 1 high side output. Low side drivers can tolerate up to -600 V below input signal (VSS: input supply return). High side driver can tolerate up to 600 V above low side ground (COM: low side supply return).
The IRS21952 has better propagation delay and thermal characteristics compared to a photo-coupler driver. The logic inputs are compatible with standard CMOS or LSTTL output. Proprietary HVIC and latch-up immune CMOS technologies enable ruggedized monolithic construction.

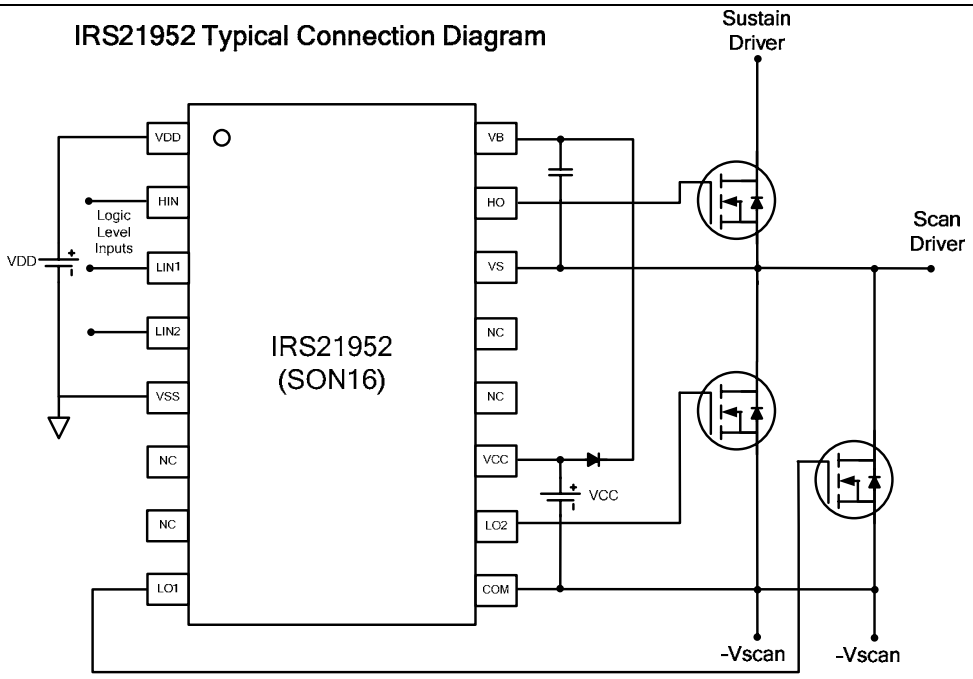
Product Summary

V_{OFFSET} (low side)	-600 V (VSS)
V_{OFFSET} (high side)	600 V (COM)
V_{OUT}	10 V to 20 V
t_{on}/t_{off} (typ)	330 ns/330 ns
$I_{o+/-}$	0.5 A/0.5 A

Package

16-Lead SOIC (narrow body)

Typical Connection Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

Symbol	Definition	Min	Max	Units
HIN LIN1 LIN2	Floating logic level input voltage	VSS-0.3	VDD+0.3	V
VDD	Floating logic input supply voltage	-0.3	625	
VSS	Floating logic input supply return voltage	VDD-25	VDD+0.3	
VB	High side floating well supply voltage	-0.3	625	
VS	High side floating well supply return voltage	VB-25	VB+0.3	
HO	High side floating gate drive output voltage	VS-0.3	VB+0.3	
VCC	Low side supply voltage	-0.3	25	
LO1 LO2	Low side output voltage	-0.3	VCC+0.3	
dVS/dt	Allowable VS offset transient relative to earth ground	-	50	V/ns
dVSS/dt	Allowable VSS offset transient relative to earth ground	-	50	V/ns
P_D	Package power dissipation @ T_A<=+25 ºC	-	1	W
$R_{\theta JA}$	Thermal resistance, junction to ambient	-	100	ºC/W
T_J	Junction temperature	-55	150	ºC
T_S	Storage temperature	-55	150	ºC
T_L	Lead temperature (soldering, 10 seconds)	-	300	ºC

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM.

Symbol	Definition	Min	Max	Units
HIN LIN1 LIN2	Floating logic level input voltage	VSS	VDD	V
VDD	Floating logic input supply voltage	VSS+4.5	VSS+5.5	
VSS	Floating logic input supply return voltage	-5	600	
VB	High side floating well supply voltage	VS+10	VS+20	
VS	High side floating well supply return voltage	-5	600	
HO	High side floating gate drive output voltage	VS	VB	
VCC	Low side supply voltage	10	20	
LO1 LO2	Low side output voltage	0	VCC	
T_A	Ambient temperature	-40	125	ºC

Note 1: Logic operation for V_S of –5 V to 600 V. Logic state held for V_S of –5 V to $–V_{BS}$. (Please refer to Design Tip DT97-3 for more details).

Static Electrical Characteristics

(VB-VS)=15 V. The V_{IN}, $V_{IN,TH}$, V_{BSUV}, V_O, I_O and I_{IN} parameters are referenced to V_S. T_A = 25 ^oC unless otherwise specified.

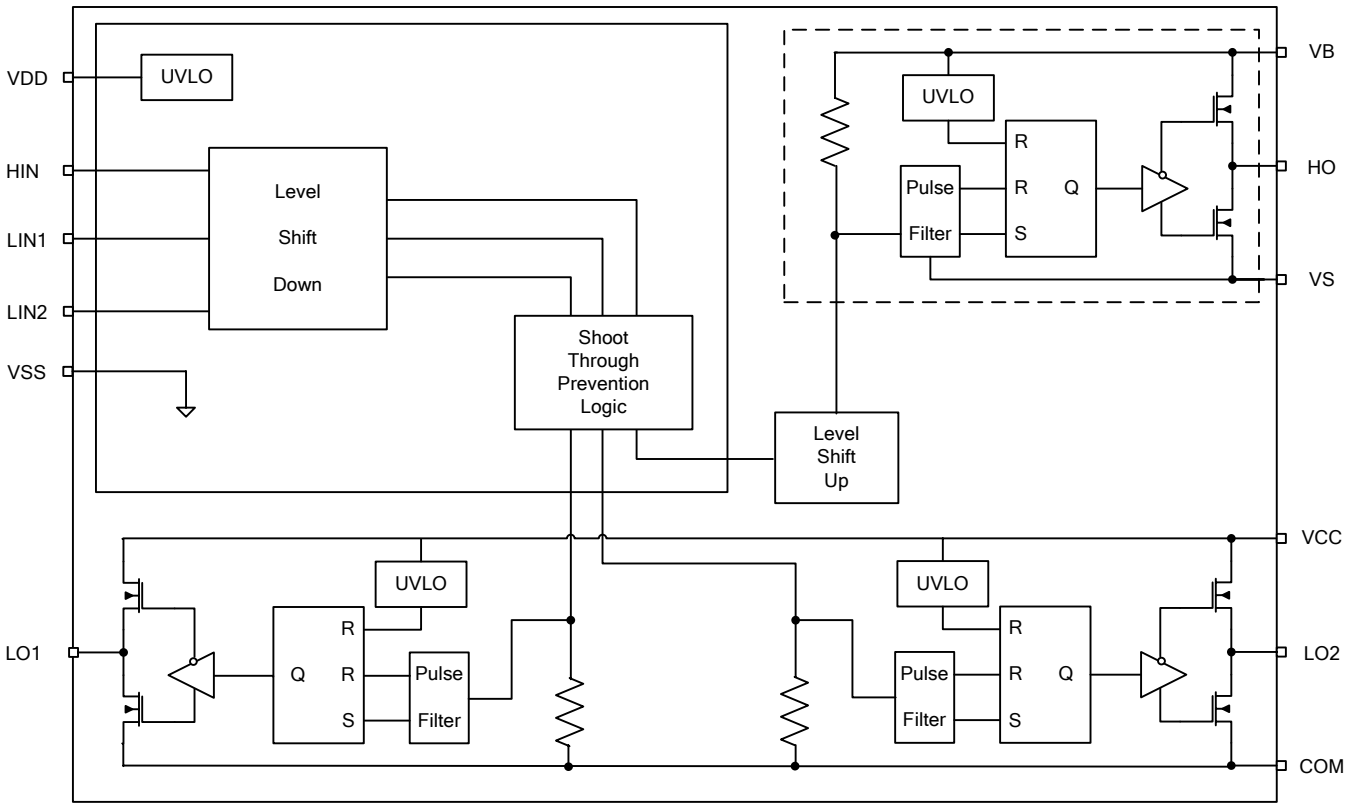
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.5	8.6	9.7	V	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.0	8.2	9.4		
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.5	8.6	9.7		
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.2	9.4		
V_{DDUV+}	V_{DD} supply undervoltage positive going threshold	3.3	4.1	4.9		
V_{DDUV-}	V_{DD} supply undervoltage negative going threshold	2.9	3.7	4.5		
I_{LKVCC} I_{LKVBS}	Offset supply leakage current – both input well and output well	---	---	50	µA	$V_B = V_S$ = 600 V $V_{CC} = V_{COM}$ = 600 V
I_{QBS}	Quiescent V_{BS} supply current	---	70	140		VIN = 0 V or 5 V
I_{QDD}	Quiescent V_{DD} supply current	---	140	280		
I_{QCC}	Quiescent V_{CC} supply current	---	200	400		
V_{IH}	Logic “1” input voltage	3.5	---	---	V	
V_{IL}	Logic “0” input voltage	---	---	0.6		
V_{OH}	High level output voltage, V_{BIAS}-V_O	---	---	0.1		I_o= 0 A
V_{OL}	Low level output voltage, V_O	---	---	0.1		I_o= 0 A
I_{IN+}	Logic “1” input bias current	---	2	10	µA	VIN = 5 V
I_{IN-}	Logic “0” input bias current	---	---	5		VIN = 0 V
I_{o+}	Output high short circuit pulsed current	---	0.5	---	A	V_O=0 V,V_{IN}=0 V, PW<=10 µs
I_{o-}	Output low short circuit pulsed current	---	0.5	---		V_O=15 V,V_{IN}=5 V, PW<=10 µs

Dynamic Electrical Characteristics (All values are target data)

(VB-VS)= 15 V. C_L = 1000 pF unless otherwise specified. All parameters are reference to COM. T_A = 25 ^oC unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay of high and low side	---	330	---	ns	V_{SS}=200 V, V_S=0 V
t_{off}	Turn-off propagation delay of high and low side	---	330	---		V_{SS}=200 V, V_S=400 V
t_r	Turn-on rise time of high and low side	---	25	70		V_{SS}=200 V, V_S=0 V
t_f	Turn-off fall time of high and low side	---	25	70		V_{ss}=200 V, V_s=400 V
MT_on	Turn on propagation delay matching	---	---	50		V_{ss}=200 V, V_s=0 V
MT_off	Turn off propagation delay matching	---	---	50		V_{ss}=200 V, V_s=400 V

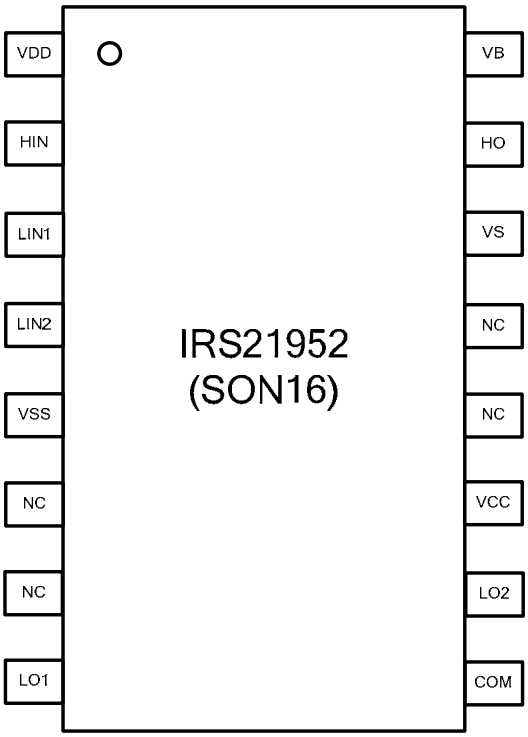
Functional Block Diagram



Lead Definitions

Symbol	Description
VDD	Input logic supply voltage
HIN	Logic input for high side gate driver
LIN1, LIN2	Logic inputs for low side gate driver
VSS	Input logic supply return
LO1, LO2	Low side outputs
VCC	Low side supply voltage
COM	Low side supply return
HO	High side output
VB	High side floating supply voltage
VS	High side floating supply return

Lead Assignments



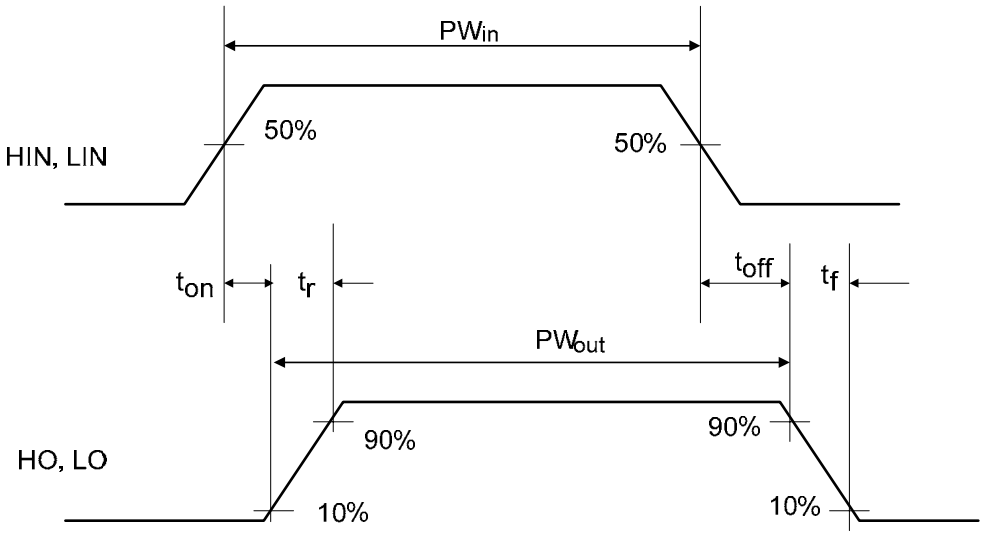


Figure 1: Switching Time Waveforms

Shoot Through Prevention Logic

HIN1	LIN1	LIN2	HO1	LO1	LO2
1	0	0	1	0	0
0	1	0	0	1	0
0	0	1	0	0	1
1	1	0	0	0	0
1	0	1	0	0	0
0	1	1	0	1	1
1	1	1	0	0	0
0	0	0	0	0	0

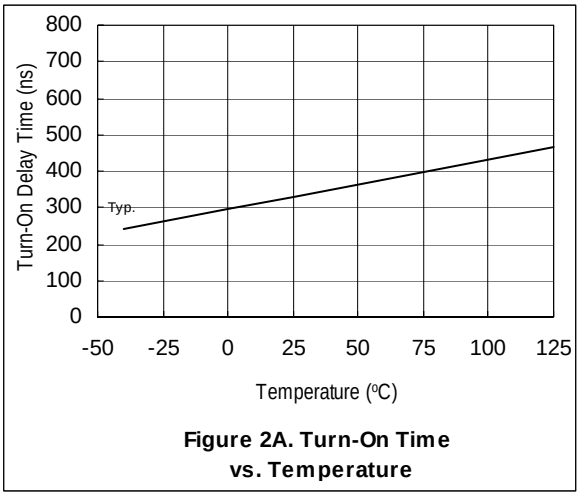


Figure 2A. Turn-On Time vs. Temperature

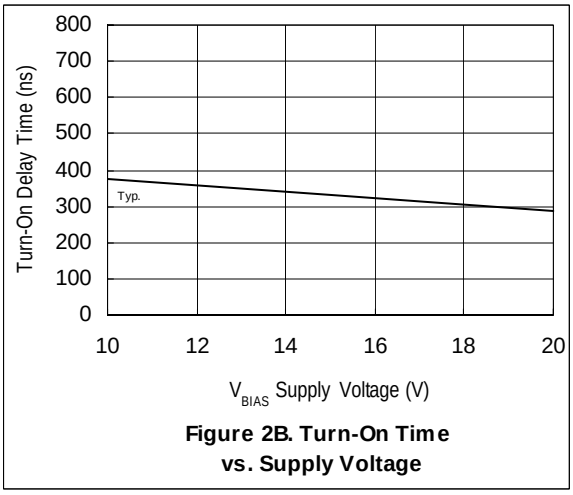


Figure 2B. Turn-On Time vs. Supply Voltage

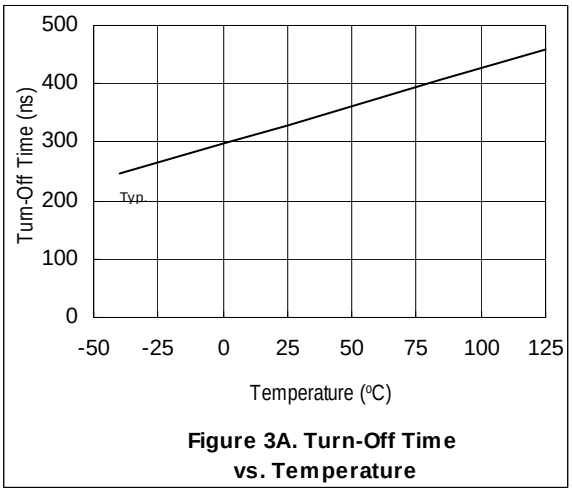


Figure 3A. Turn-Off Time vs. Temperature

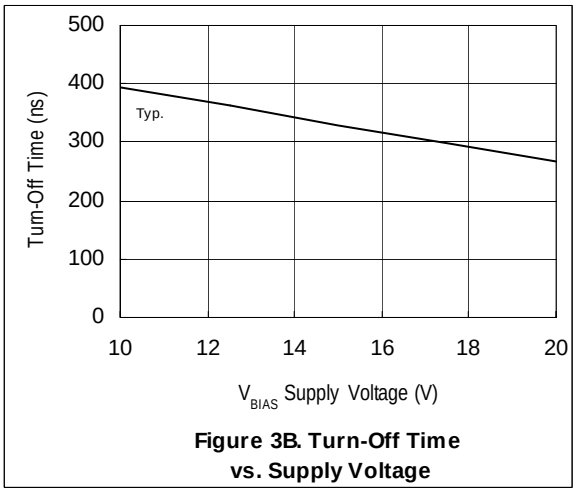
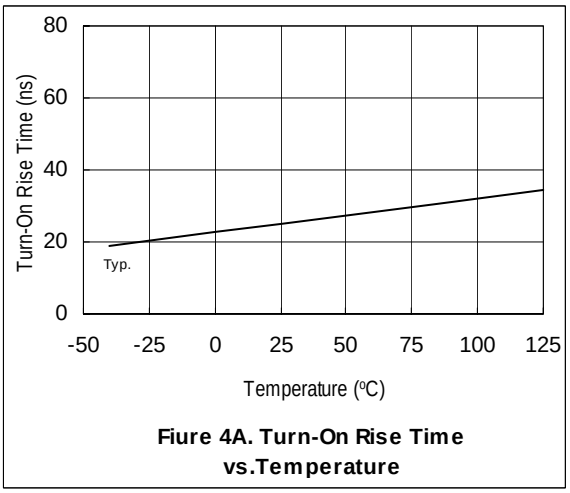


Figure 3B. Turn-Off Time vs. Supply Voltage



Fiure 4A. Turn-On Rise Time vs.Temperature

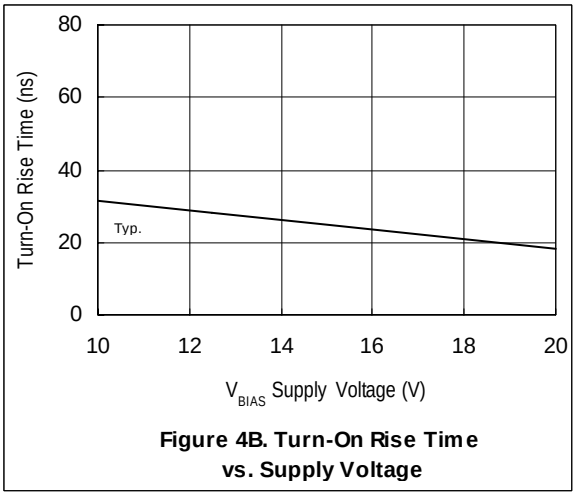


Figure 4B. Turn-On Rise Time vs. Supply Voltage

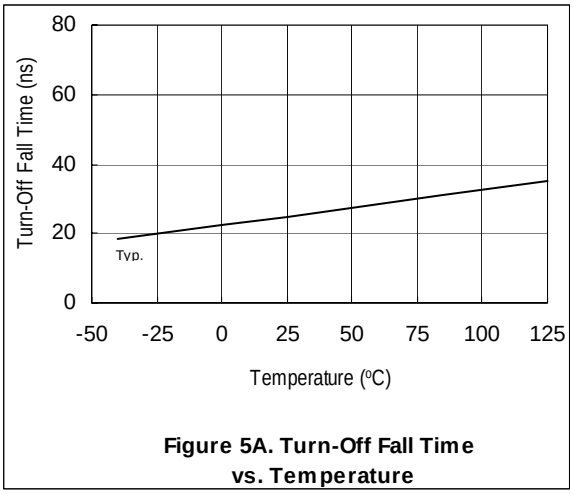


Figure 5A. Turn-Off Fall Time vs. Temperature

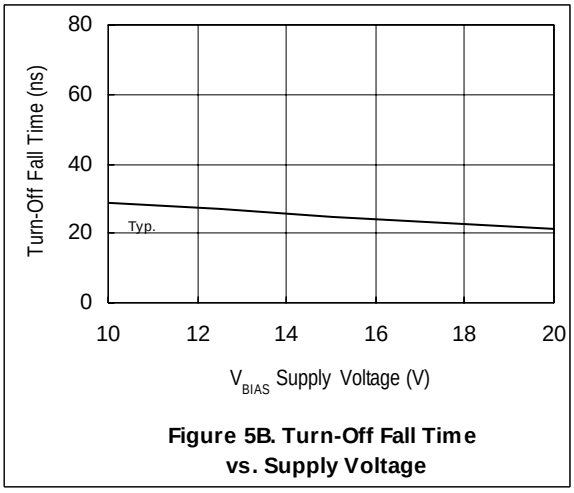


Figure 5B. Turn-Off Fall Time vs. Supply Voltage

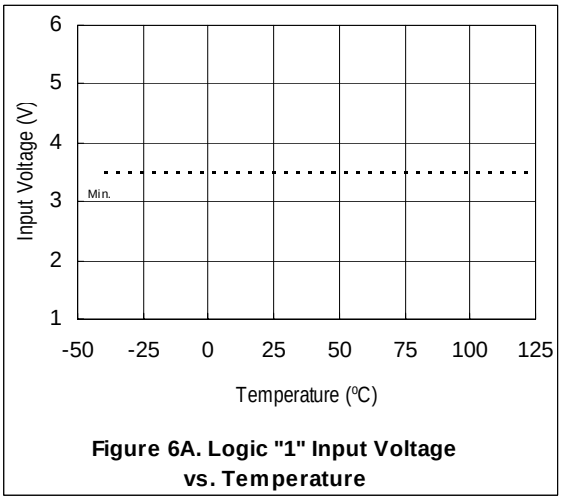


Figure 6A. Logic "1" Input Voltage vs. Temperature

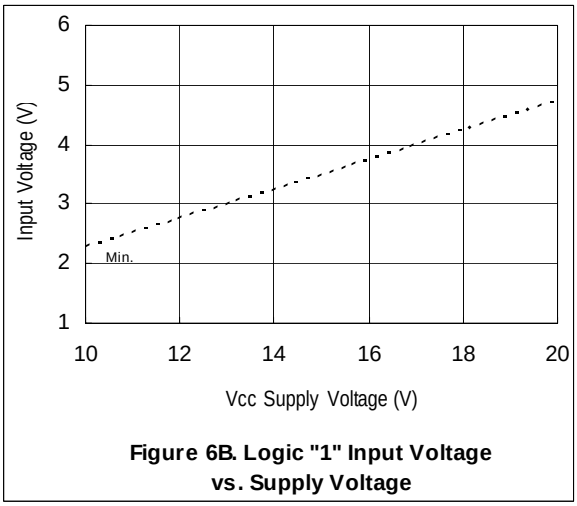


Figure 6B. Logic "1" Input Voltage vs. Supply Voltage

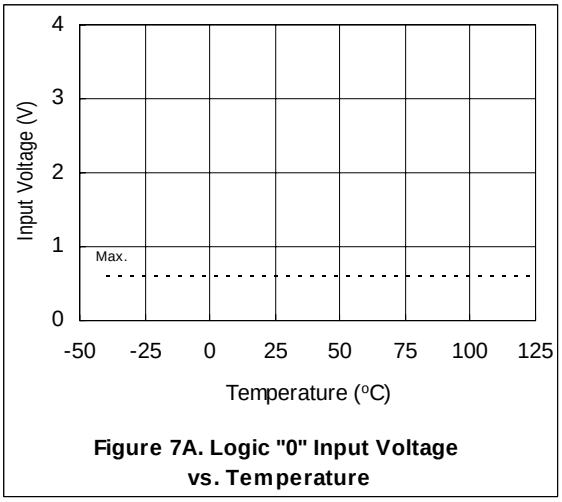


Figure 7A. Logic "0" Input Voltage vs. Temperature

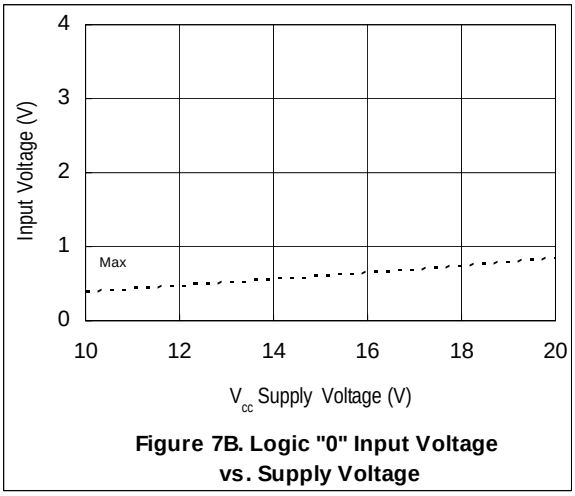


Figure 7B. Logic "0" Input Voltage vs. Supply Voltage

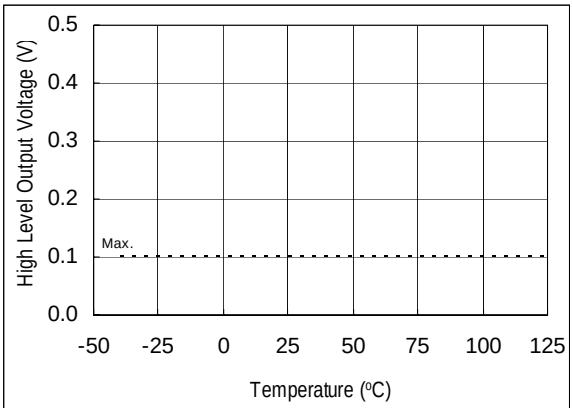


Figure 8A. High Level Output vs. Temperature

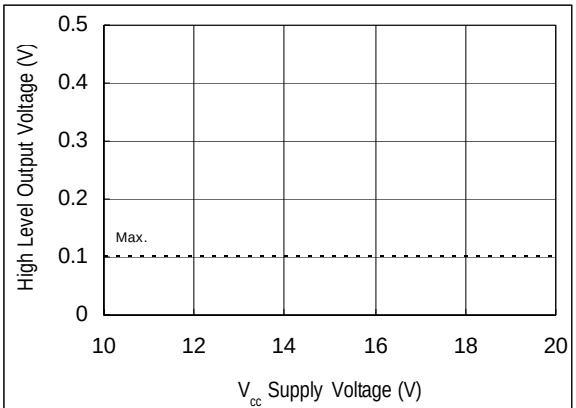


Figure 8B. High Level Output vs. Supply Voltage

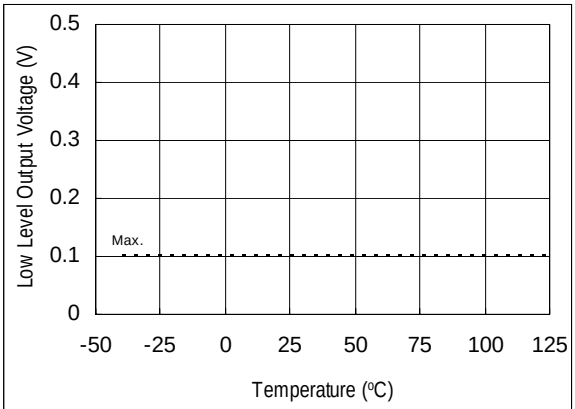


Figure 9A. Low Level Output vs.Temperature

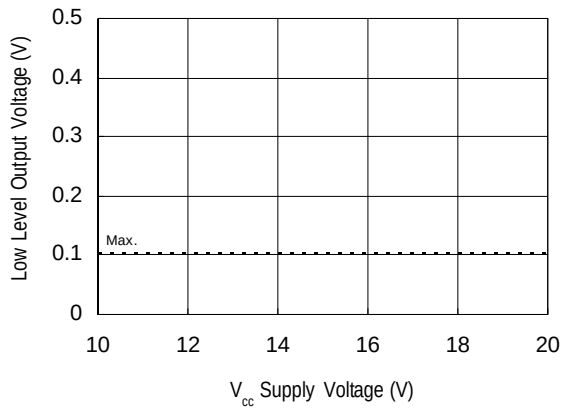


Figure 9B. Low Level Output vs. Supply Voltage

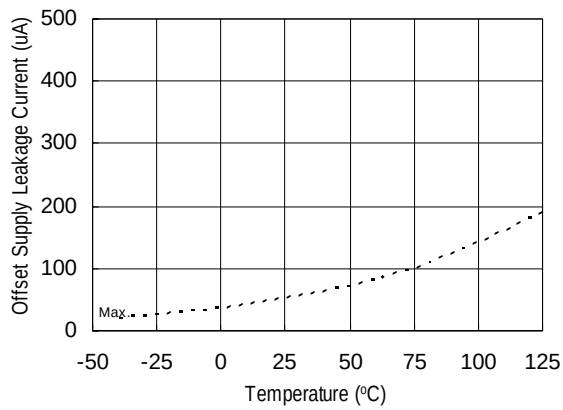


Figure 10A. Offset Supply Leakage Current vs. Temperature

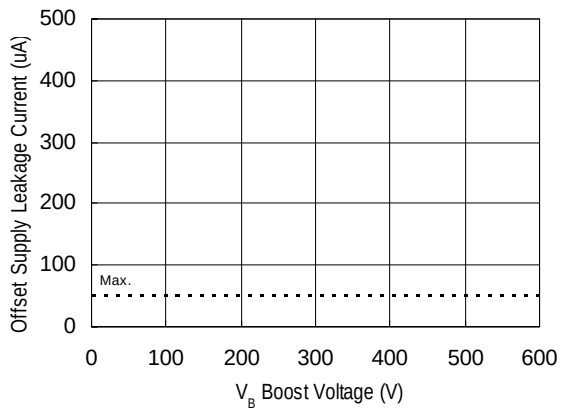


Figure 10B. Offset Supply Leakage Current vs. Supply Voltage

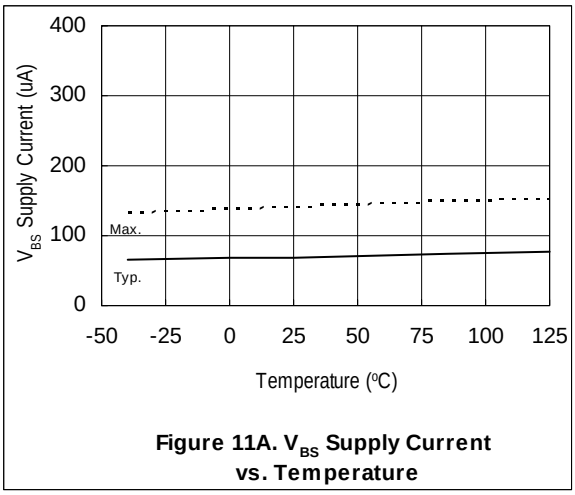


Figure 11A. V_{BS} Supply Current vs. Temperature

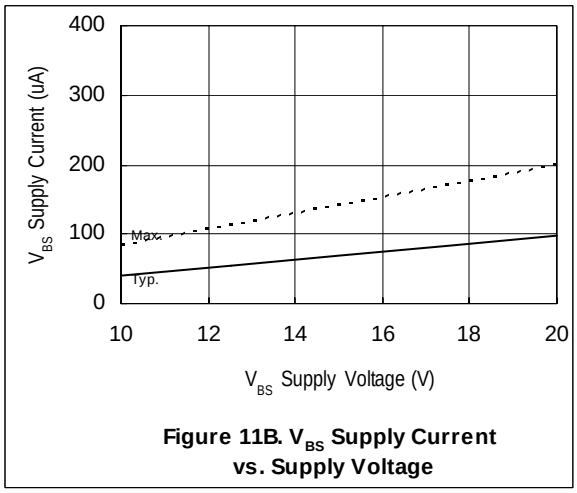


Figure 11B. V_{BS} Supply Current vs. Supply Voltage

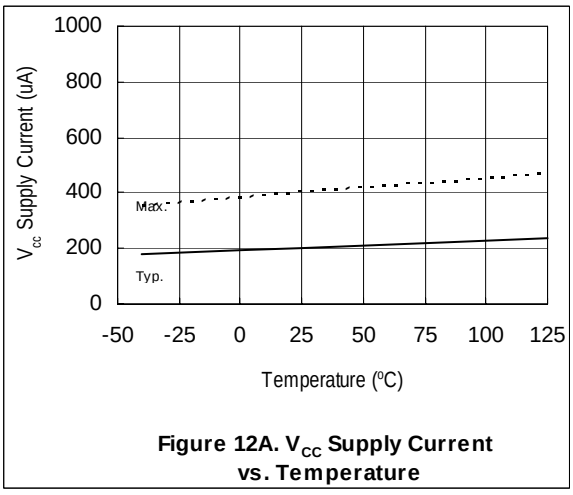


Figure 12A. V_{CC} Supply Current vs. Temperature

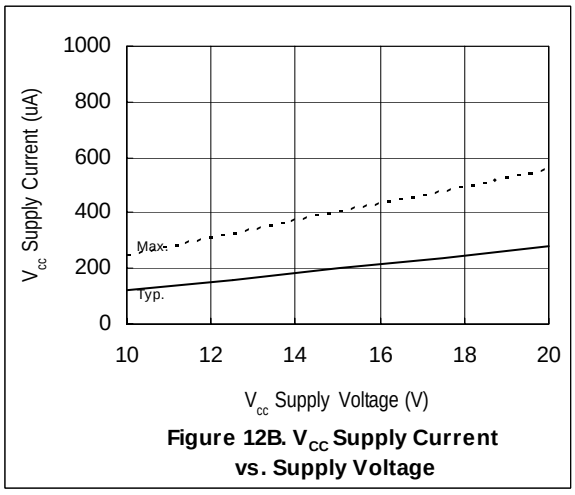


Figure 12B. V_{CC} Supply Current vs. Supply Voltage

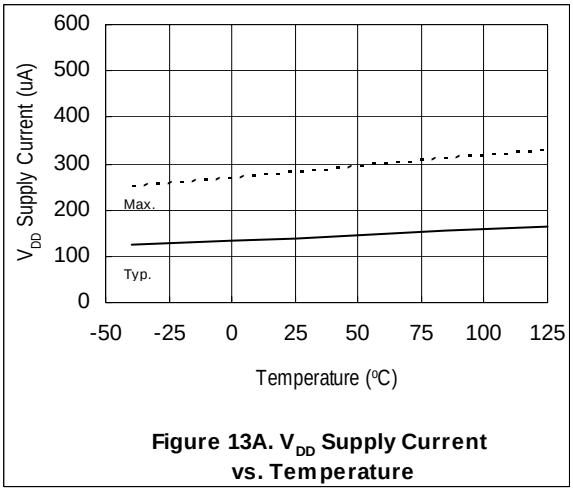


Figure 13A. V_{DD} Supply Current vs. Temperature

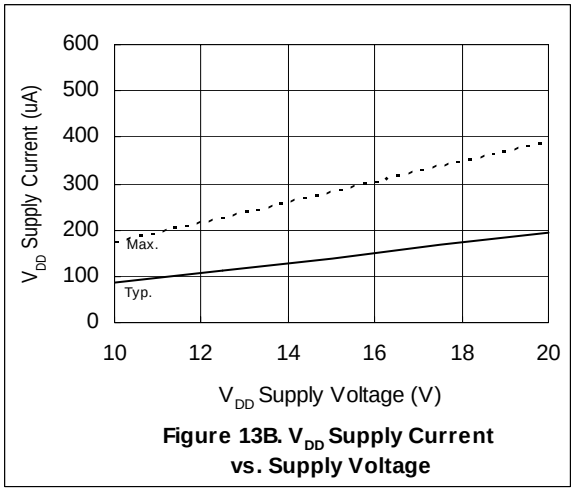


Figure 13B. V_{DD} Supply Current vs. Supply Voltage

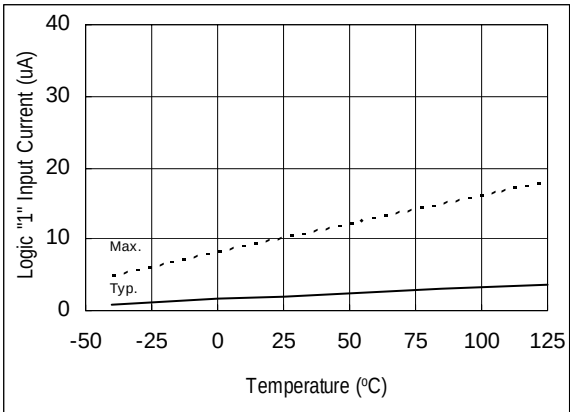


Figure 14A. Logic "1" Input Current vs. Temperature

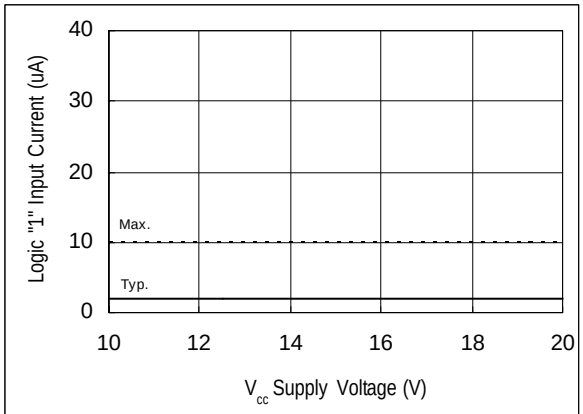


Figure 14B. Logic "1" Input Current vs. Supply Voltage

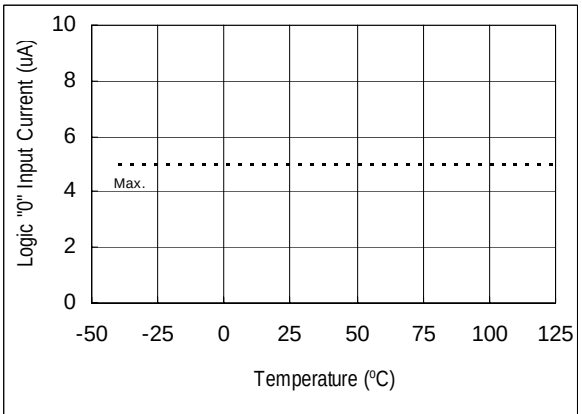


Figure 15A. Logic "0" Input Current vs. Temperature

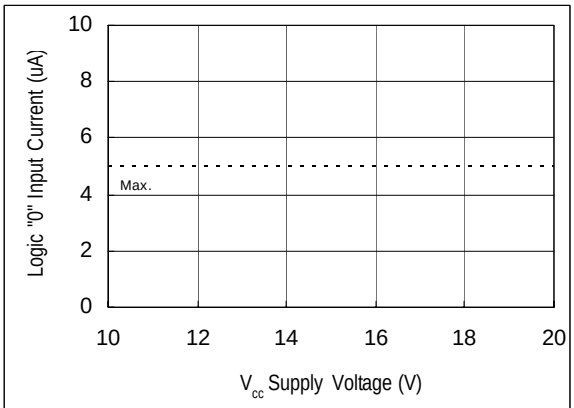


Figure 15B. Logic "0" Input Current vs. Supply Voltage

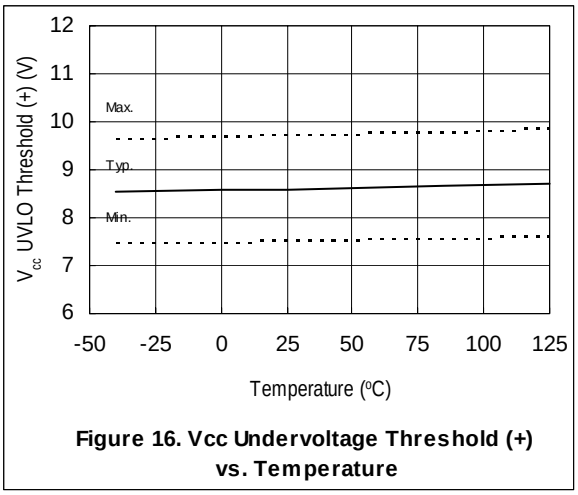


Figure 16. Vcc Undervoltage Threshold (+) vs. Temperature

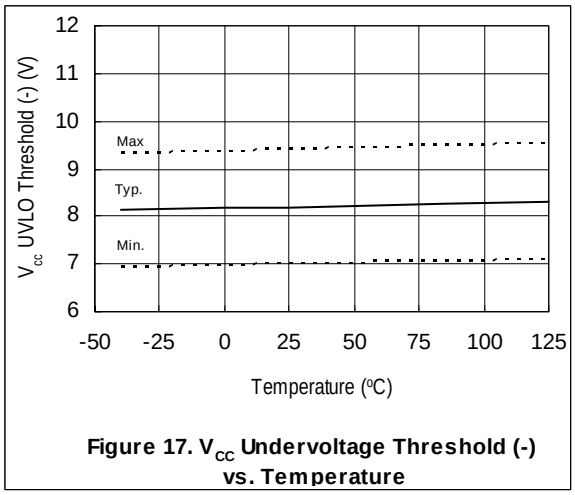


Figure 17. V_{CC} Undervoltage Threshold (-) vs. Temperature

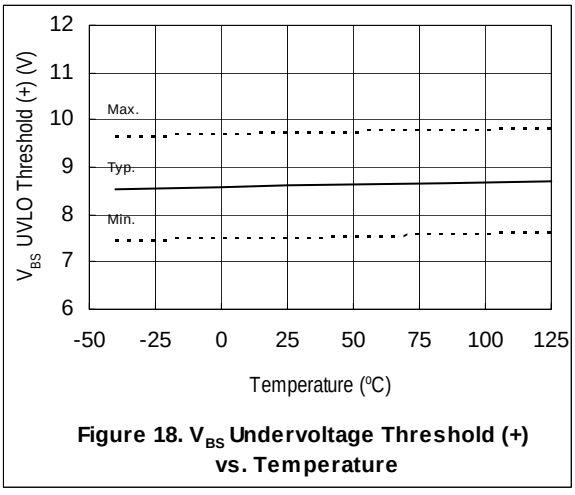


Figure 18. V_{BS} Undervoltage Threshold (+) vs. Temperature

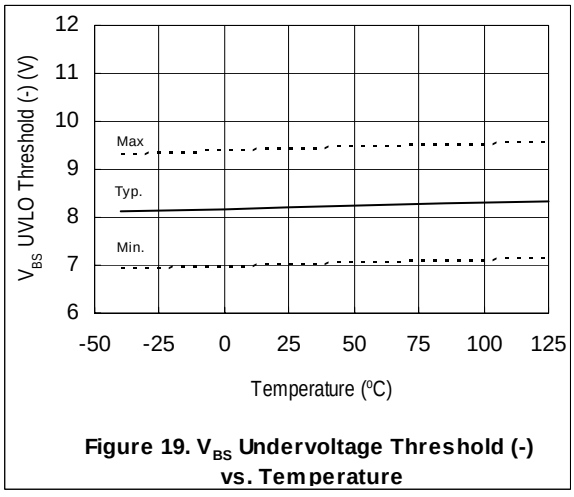


Figure 19. V_{BS} Undervoltage Threshold (-) vs. Temperature

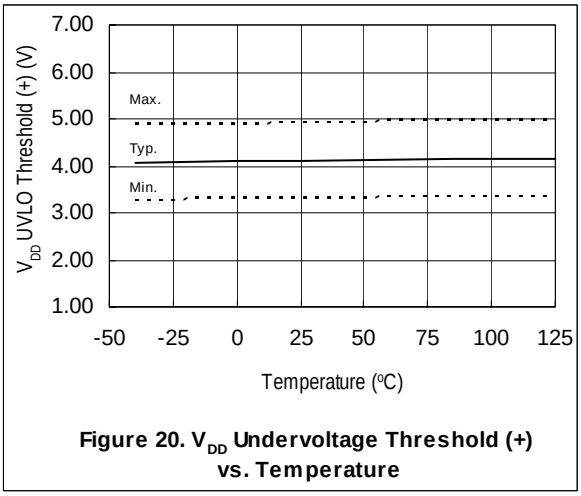


Figure 20. V_{DD} Undervoltage Threshold (+) vs. Temperature

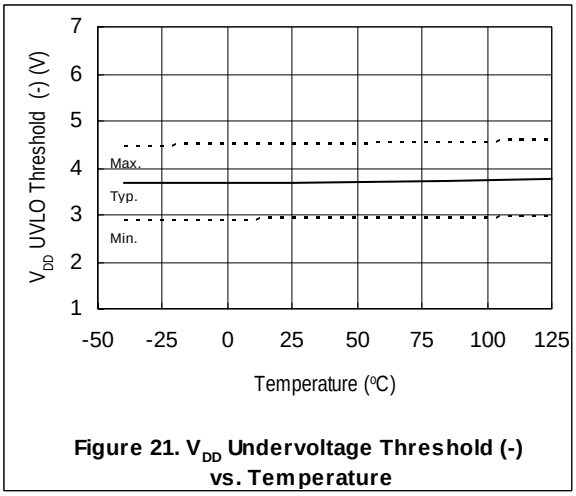


Figure 21. V_{DD} Undervoltage Threshold (-) vs. Temperature

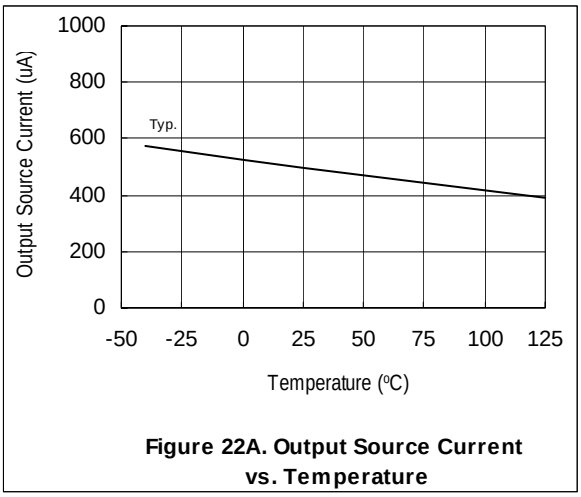


Figure 22A. Output Source Current vs. Temperature

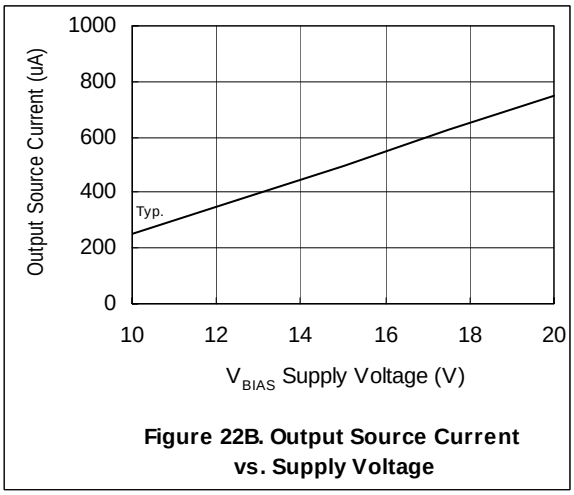


Figure 22B. Output Source Current vs. Supply Voltage

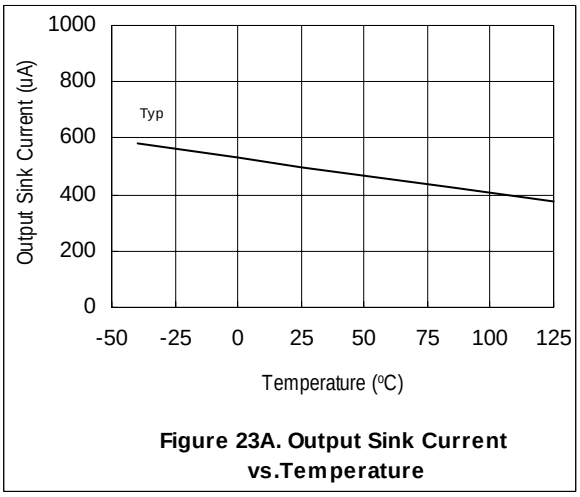


Figure 23A. Output Sink Current vs.Temperature

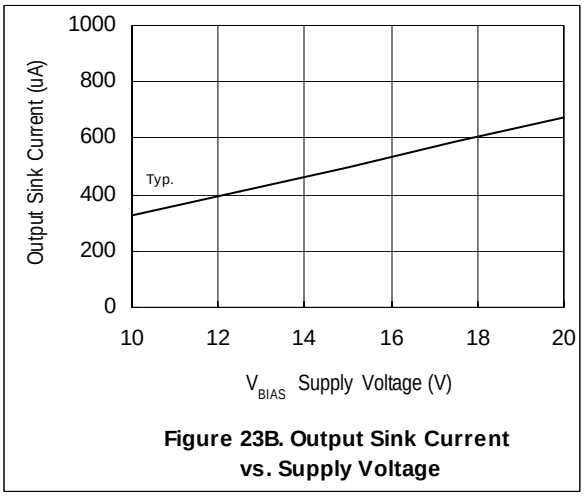


Figure 23B. Output Sink Current vs. Supply Voltage

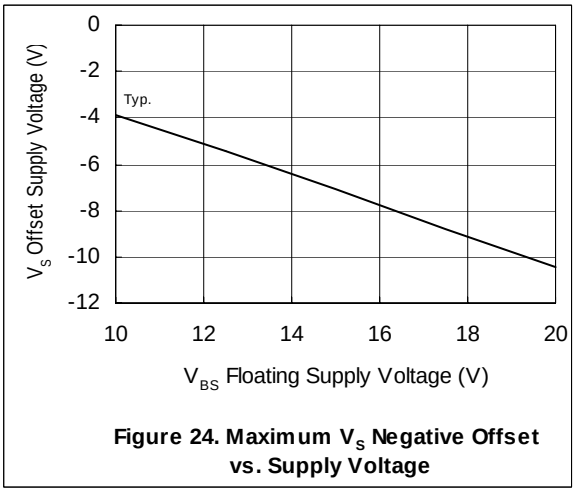
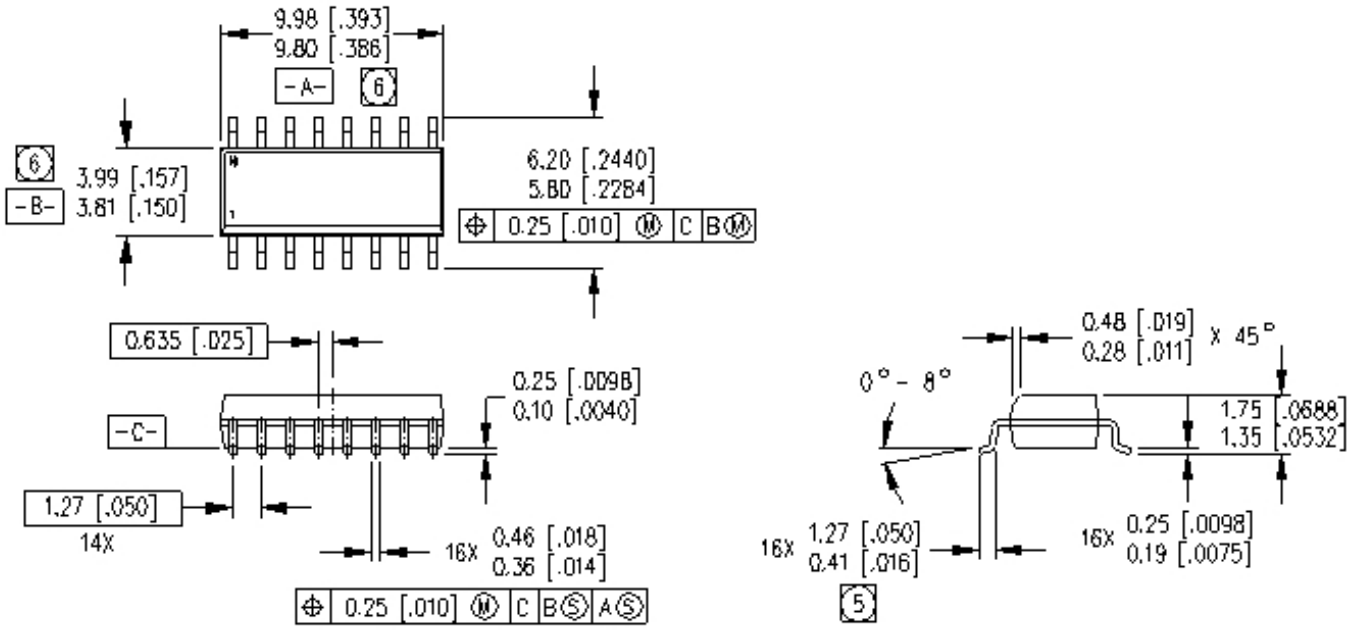


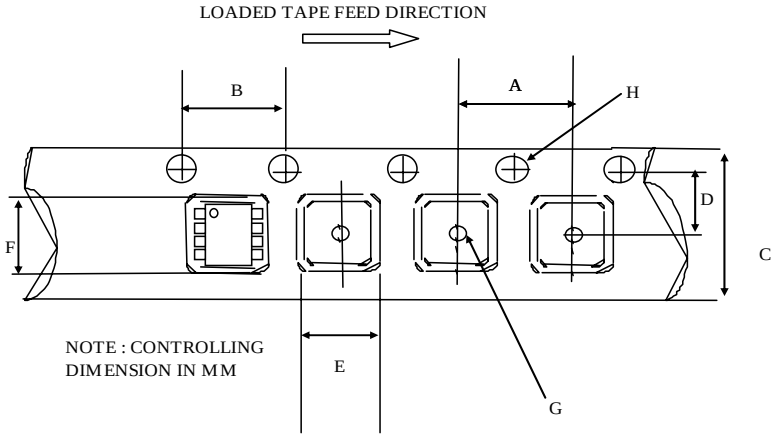
Figure 24. Maximum V_S Negative Offset vs. Supply Voltage



NOTES:

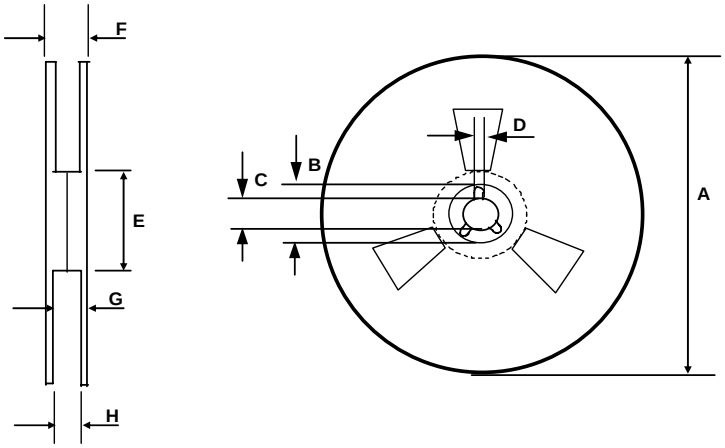
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5W-1982
2. CONTROLLING DIMENSION. MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETER [INCHES]
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006]

16-Lead SOIC (narrow body)



CARRIER TAPE DIMENSION FOR 16SOICN

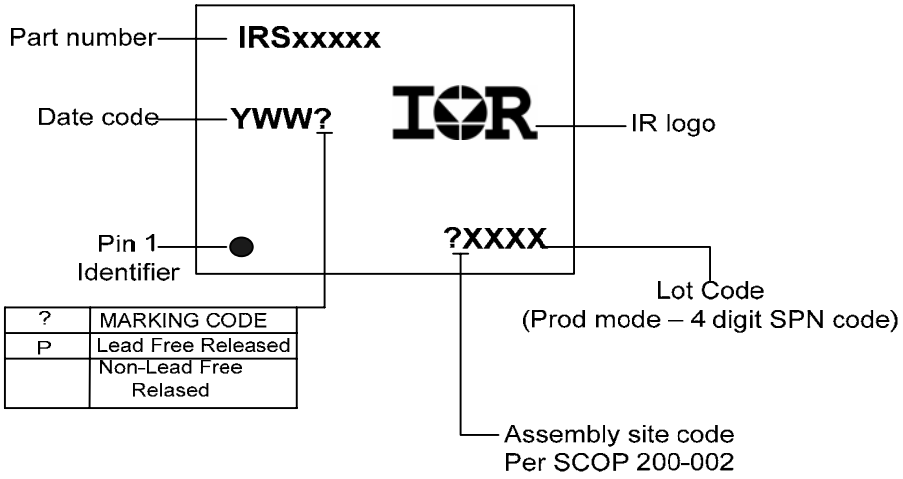
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	10.20	10.40	0.402	0.409
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

LEAD-FREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

ORDER INFORMATION

16-Lead SOIC IRS21952SPBF

16-Lead SOIC Tape & Reel IRS21952STRPBF