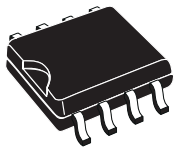
STS7C4F30L

N-CHANNEL 30V - 0.018 Ω - 7A SO-8
P-CHANNEL 30V - 0.070 Ω - 4A SO-8
STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STS7C4F30L(N-Channel)	30 V	<0.022 Ω	7 A
STS7C4F30L(P-Channel)	30 V	<0.080 Ω	4 A

- TYPICAL R_{DS}(on) (N-Channel) = 0.018 Ω
- TYPICAL R_{DS}(on) (P-Channel) = 0.070 Ω
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE



SO-8

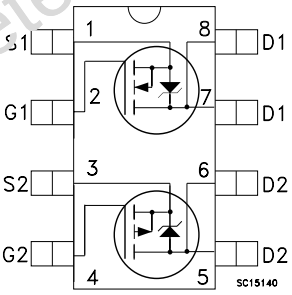
DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC/DC CONVERTERS
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	N-CHANNEL	P-CHANNEL	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	30	V
V_{GS}	Gate- source Voltage	± 20	± 20	V
I_D	Drain Current (continuos) at T_C = 25°C Single Operating	7	4	A
I_D	Drain Current (continuos) at T_C = 100°C Single Operating	4.4	2.5	A
I_{DM}(•)	Drain Current (pulsed)	28	16	A
P_{tot}	Total Dissipation at T_C = 25°C Dual Operating Total Dissipation at T_C = 25°C Single Operating	1.6 2		W W
T_{stg}	Storage Temperature	-60 to 150		°C
T_j	Max. Operating Junction Temperature	150		°C

(•) Pulse width limited by safe operating area.

Note: P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

THERMAL DATA

Rthj-amb(1)	Thermal Resistance Junction-ambient	Single Operation	62.5	°C/W
		Dual Operating	78	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

(1) when mounted on 0.5 in^2 pad of 2 oz. copper

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	n-ch p-ch	30 30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C				1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V V_{GS} = ± 20V	n-ch p-ch			±100 ±100	nA nA

ON

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}	I_D = 250 µA	n-ch p-ch	1 1	1.6 1.6	2.5 2.5	V V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V V_{GS} = 10 V V_{GS} = 4.5 V V_{GS} = 4.5 V	I_D = 3.5 A I_D = 2 A I_D = 3.5 A I_D = 2 A	n-ch p-ch n-ch p-ch		0.018 0.070 0.021 0.085	0.022 0.080 0.026 0.10	Ω Ω Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} = 15 V V_{DS} = 15 V	I_D= 3.5 A I_D= 2 A	n-ch p-ch		10 10		S S
C_{iss}	Input Capacitance			n-ch p-ch		1050 1350		pF pF
C_{oss}	Output Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		n-ch p-ch		250 490		pF pF
C_{rss}	Reverse Transfer Capacitance			n-ch p-ch		85 130		pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	**N-CHANNEL** V_{DD} = 15 V I_D = 3.5 A R_G = 4.7 Ω V_{GS} = 4.5 V **P-CHANNEL** V_{DD} = 15 V I_D = 2 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, Figure 1)	n-ch p-ch n-ch p-ch		22 25 60 35		ns ns ns ns
t_r	Rise Time						
Qg	Total Gate Charge	**N-CHANNEL** V_{DD} = 24V I_D = 7A V_{GS} = 5V **P-CHANNEL** V_{DD} = 24V I_D = 4A V_{GS} = 5V (see test circuit, Figure 2)	n-ch p-ch		17.5 12.5	23 16	nC nC
Q_{gs}	Gate-Source Charge		n-ch p-ch		4 5		nC nC
Q_{gd}	Gate-Drain Charge		n-ch p-ch		7 3		nC nC

SWITCHING OFF

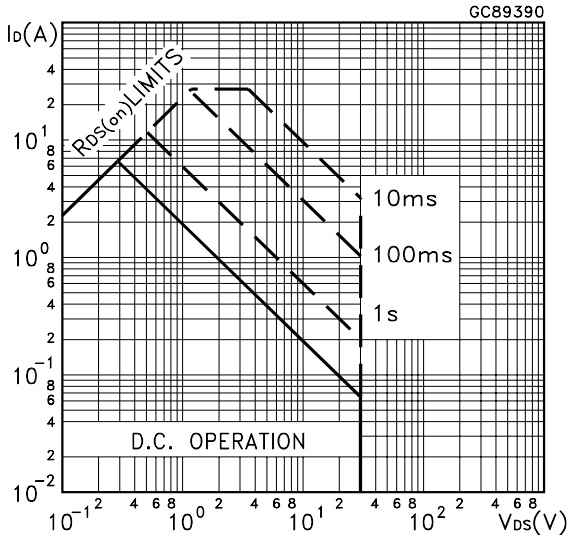
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	**N-CHANNEL** V_{DD} = 15 V I_D = 3.5 A R_G = 4.7 Ω V_{GS} = 4.5 V **P-CHANNEL** V_{DD} = 15 V I_D = 2 A R_G = 4.7 Ω V_{GS} = 4.5 V (Resistive Load, Figure 1)	n-ch p-ch n-ch p-ch		42 125 10 35		ns ns ns ns
t_f	Fall Time						

SOURCE DRAIN DIODE

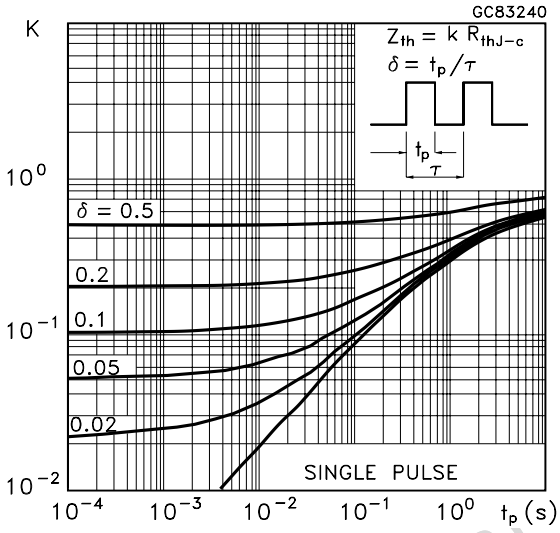
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current		n-ch p-ch			7 4	A A
I_{SDM} (•)	Source-drain Current (pulsed)		n-ch p-ch			28 16	A A
V_{SD}(*)	Forward On Voltage	I_{SD} = 7 A V_{GS} = 0 I_{SD} = 4 A V_{GS} = 0	n-ch p-ch			1.2 1.2	V V
t_{rr}	Reverse Recovery Time	**N-CHANNEL** I_{SD} = 7 A di/dt = 100A/µs V_{DD} = 15 V T_j =150 °C **P-CHANNEL** I_{SD} = 4 A di/dt = 100A/µs V_{DD} = 15 V T_j =150 °C (see test circuit, Figure 3)	n-ch p-ch n-ch p-ch n-ch p-ch		50 45 40 36 1.6 1.6		ns ns nC nC A A
Q_{rr}	Reverse Recovery Charge						
I_{RRM}	Reverse Recovery Current						

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•) Pulse width limited by safe operating area.

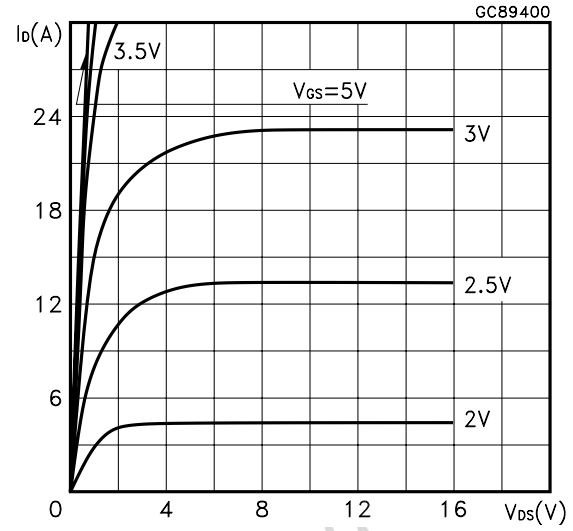
Safe Operating Area **n-ch**



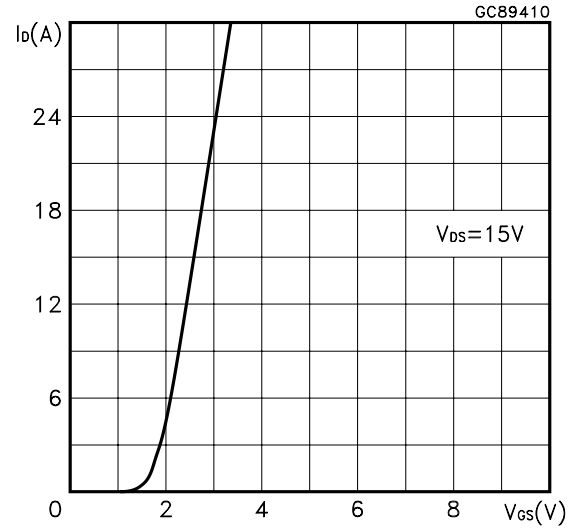
Thermal Impedance **n-ch**



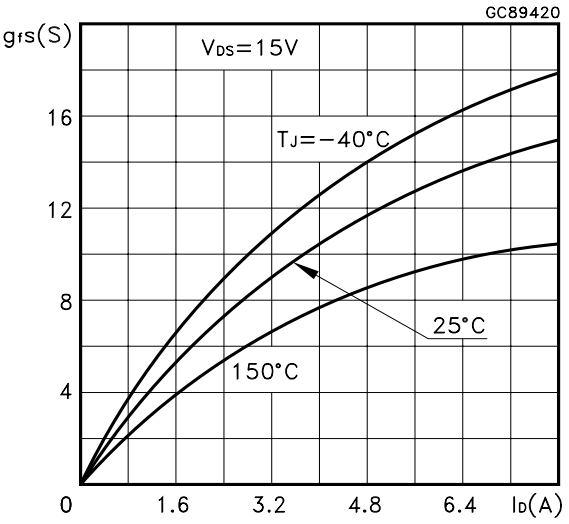
Output Characteristics **n-ch**



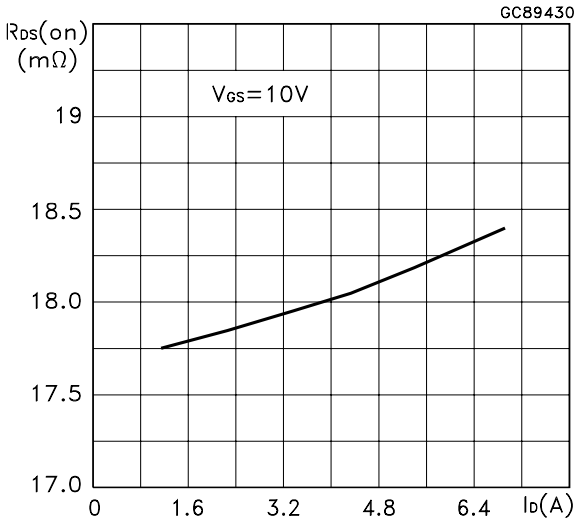
Transfer Characteristics **n-ch**



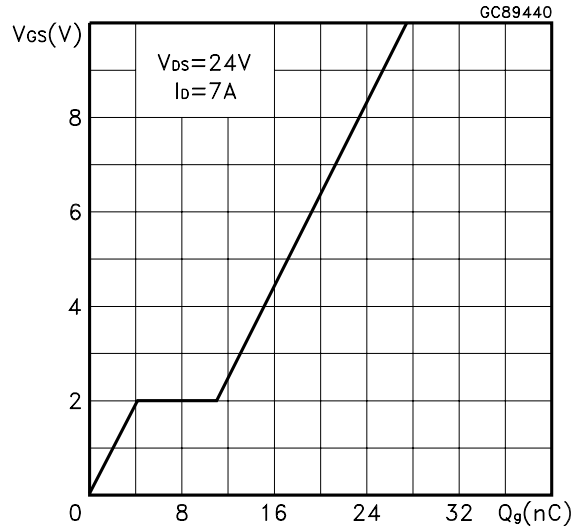
Transconductance **n-ch**



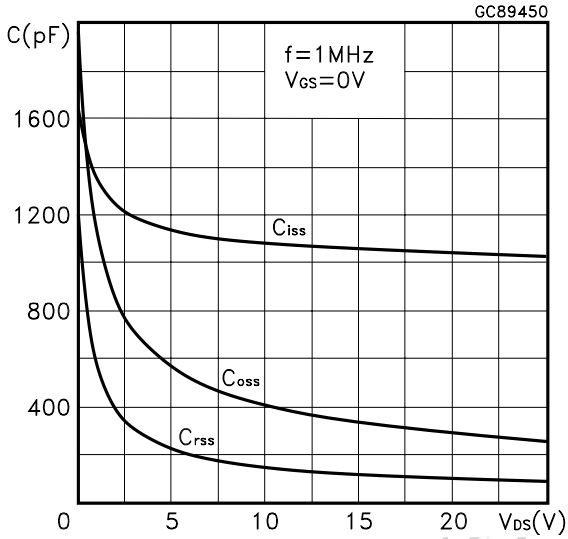
Static Drain-source On Resistance **n-ch**



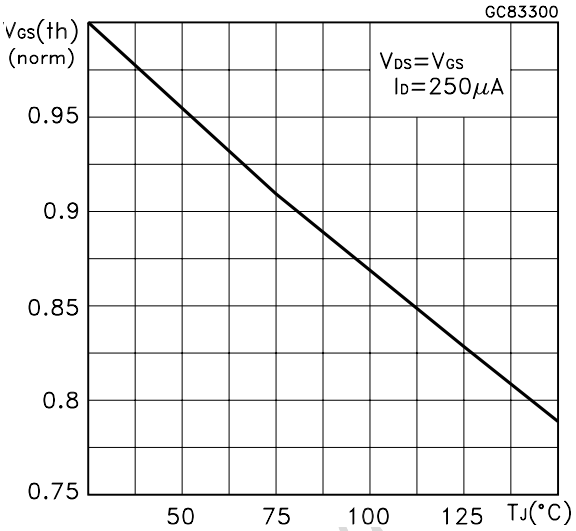
Gate Charge vs Gate-source Voltage **n-ch**



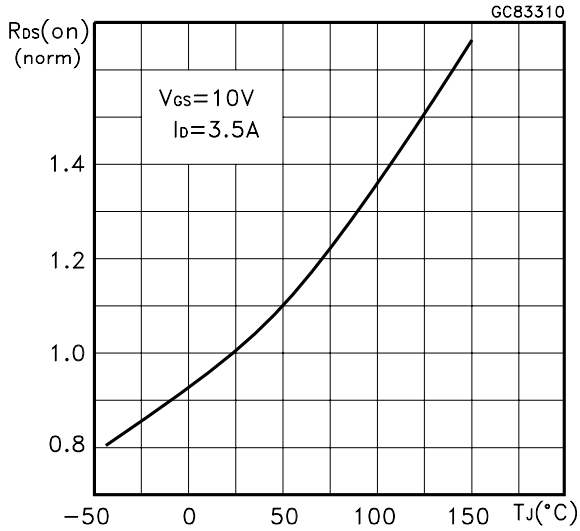
Capacitance Variations **n-ch**



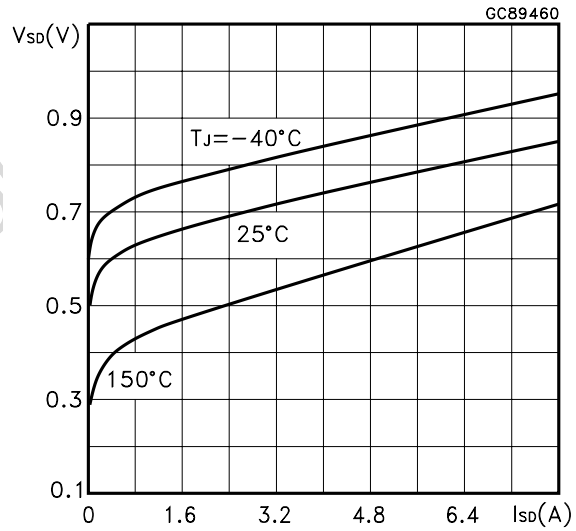
Normalized Gate Threshold Voltage vs Temperature **n-ch**



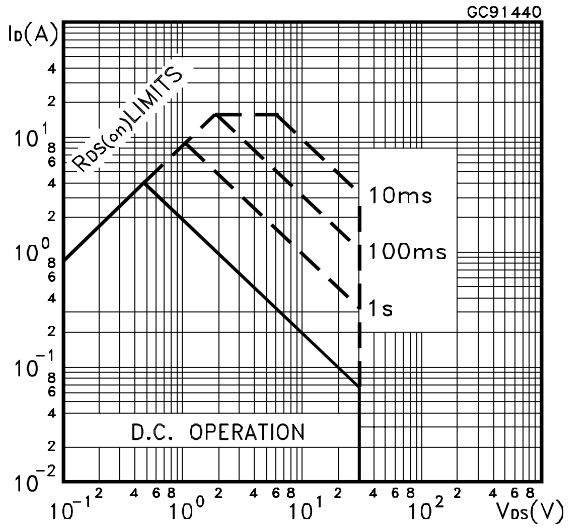
Normalized on Resistance vs Temperature **n-ch**



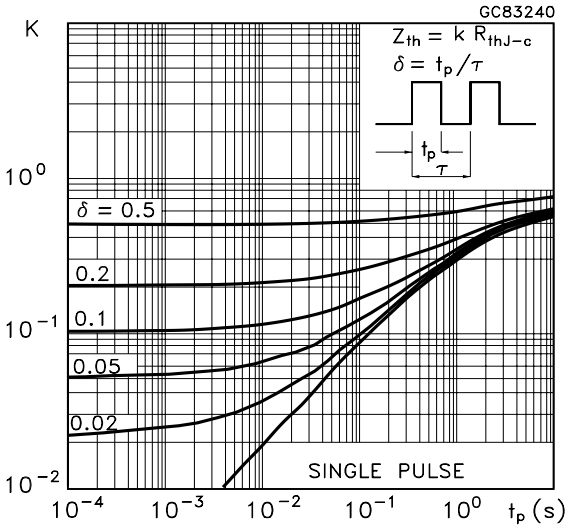
Source-drain Diode Forward Characteristics **n-ch**



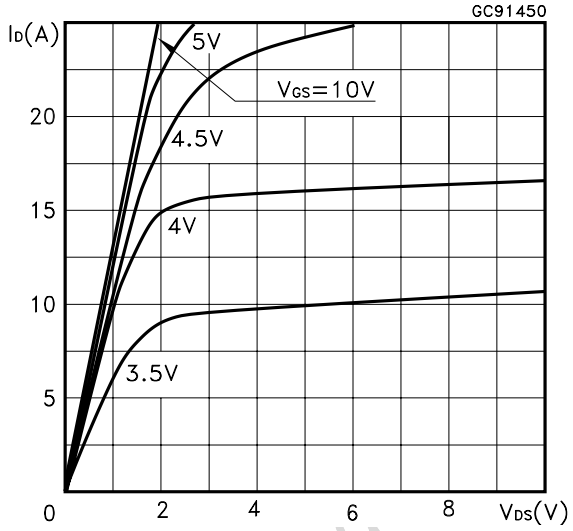
Safe Operating Area **p-ch**



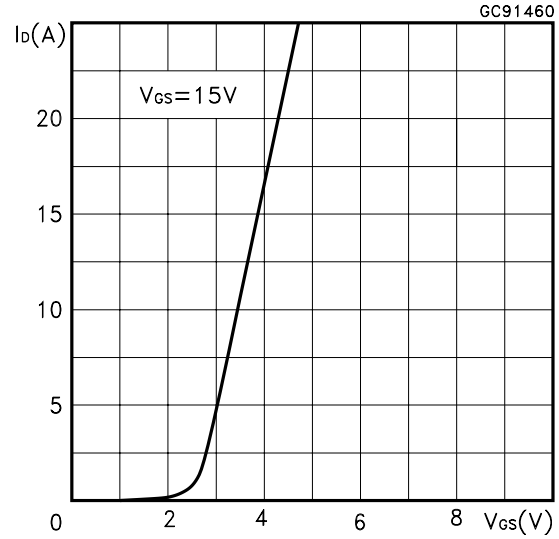
Thermal Impedance **p-ch**



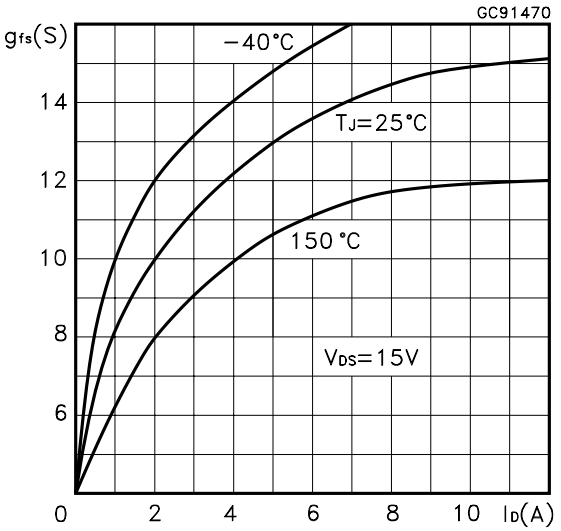
Output Characteristics **p-ch**



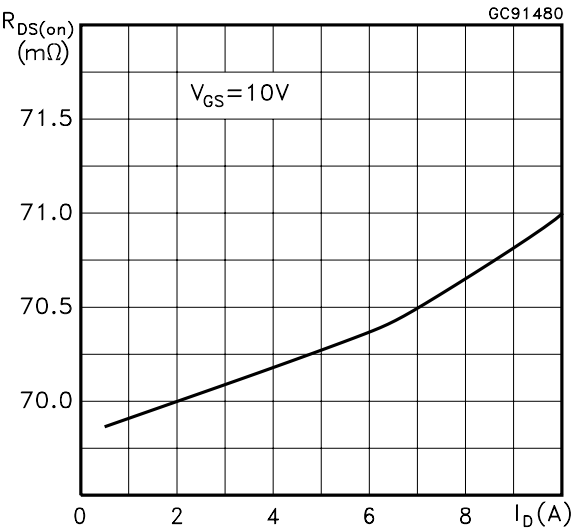
Transfer Characteristics **p-ch**



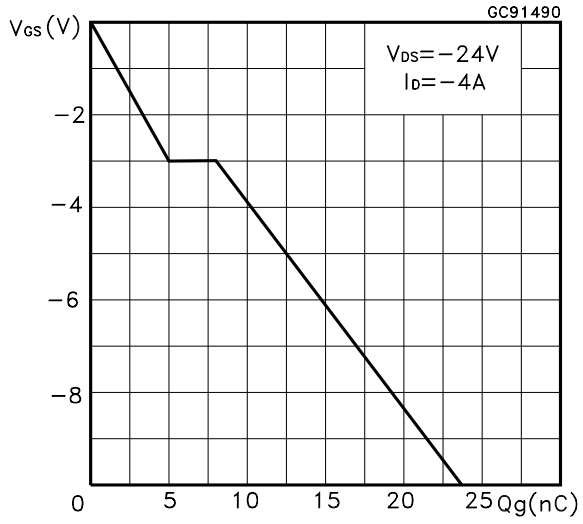
Transconductance **p-ch**



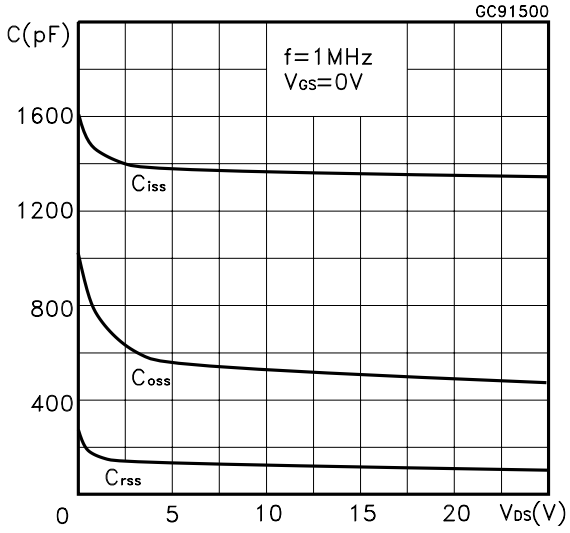
Static Drain-source On Resistance **p-ch**



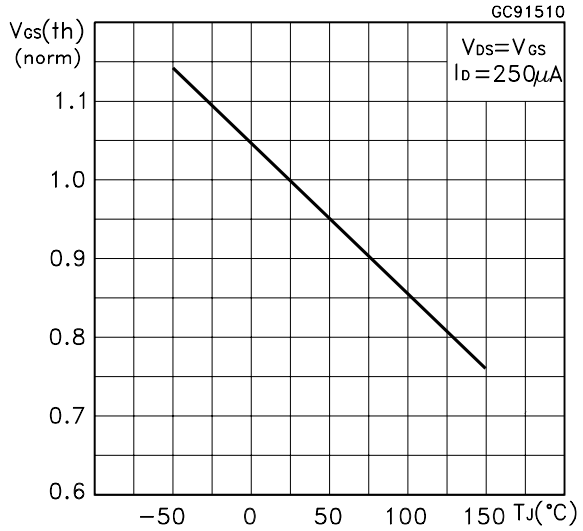
Gate Charge vs Gate-source Voltage **p-ch**



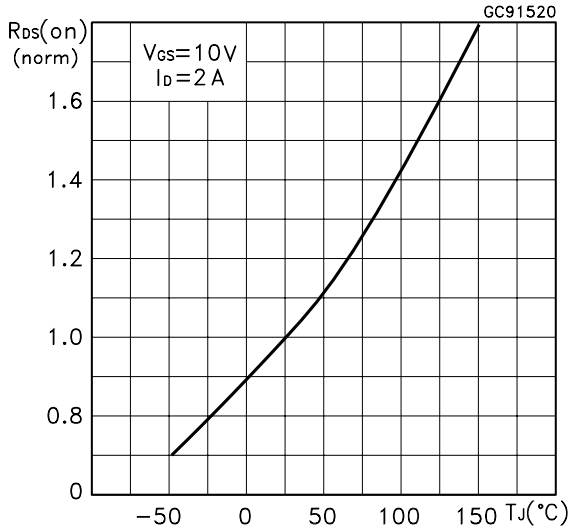
Capacitance Variations **p-ch**



Normalized Gate Threshold Voltage vs Temperature **p-ch**



Normalized on Resistance vs Temperature **p-ch**



Source-drain Diode Forward Characteristics **p-ch**

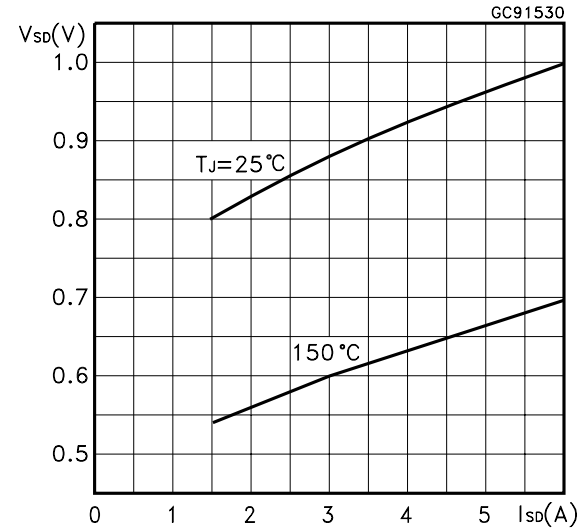


Fig. 1: Switching Times Test Circuits For Resistive Load

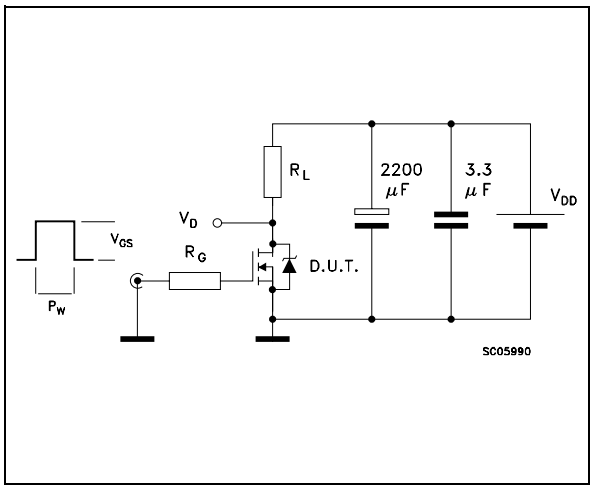


Fig. 2: Gate Charge test Circuit

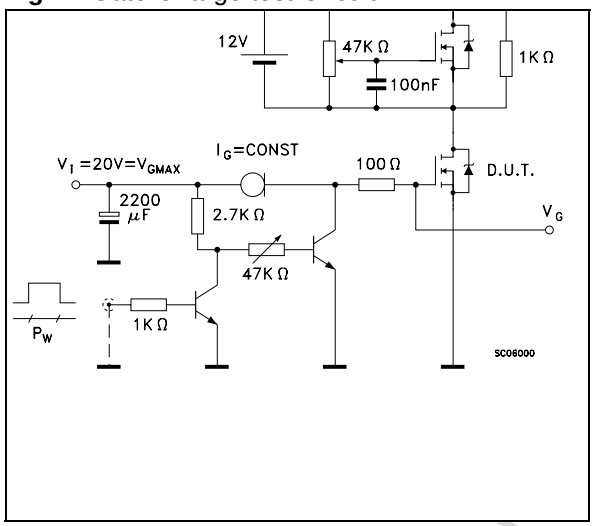
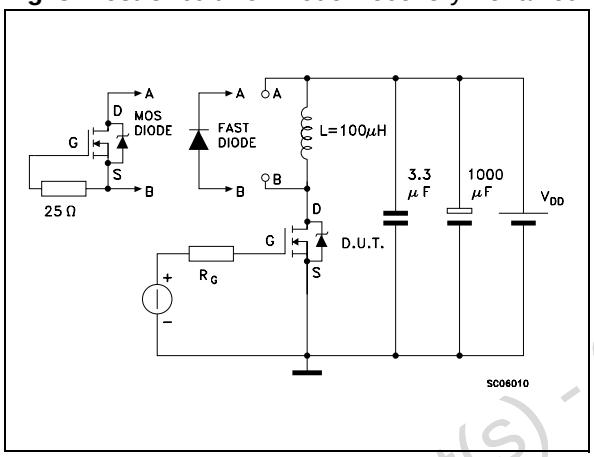
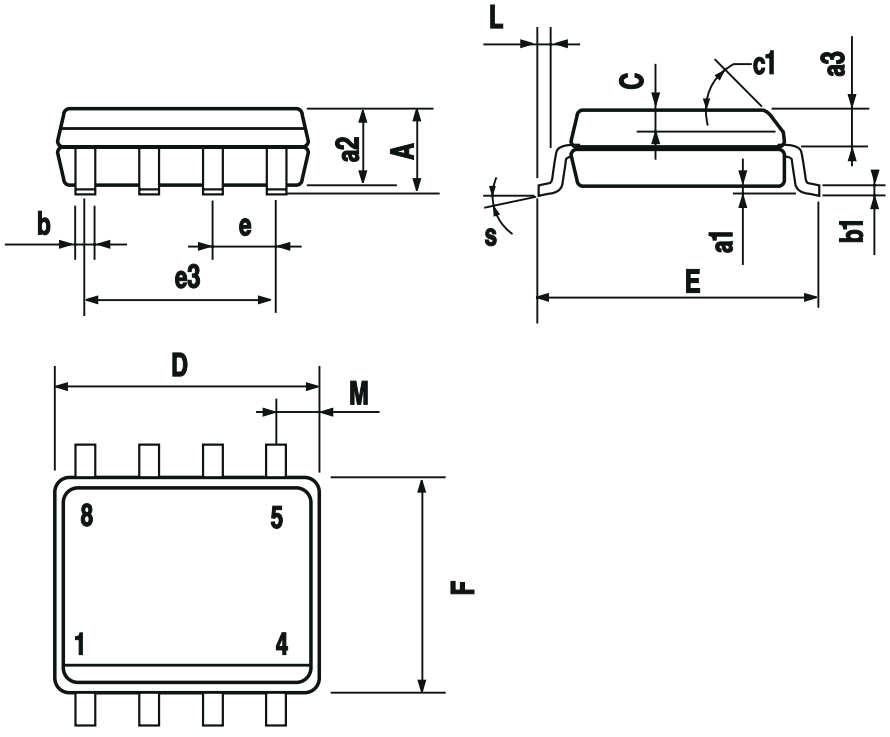


Fig. 3: Test Circuit For Diode Recovery Behaviour



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



0016023