NDPL070N10B

Power MOSFET
100V, 10.8mΩ, 70A, N-Channel

This N-Channel Power MOSFET is produced using ON Semiconductor's trench technology, which is specifically designed to minimize gate charge and ultra low on resistance. This device is suitable for applications with low gate charge driving or ultra low on resistance requirements.

ON Semiconductor®

www.onsemi.com

Features

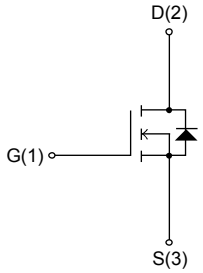
- Low On-Resistance
- Low Gate Charge
- High Speed Switching
- 100% Avalanche Tested
- Pb-Free and RoHS compliance

Applications

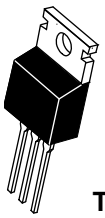
- Battery Protection
- Motor Drive
- Primary Side Switch
- Secondary Side Synchronous Rectification

V_{DSS}	R_{DS}(on) Max	I_D Max
100V	10.8 mΩ@15V	70A
	12.8 mΩ@10V	

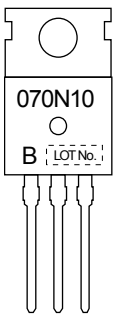
ELECTRICAL CONNECTION
N-Channel



MARKING



TO-220-3L



SPECIFICATION

ABSOLUTE MAXIMUM RATINGS at Ta = 25°C (Note 1)

Parameter	Symbol	Value	Unit
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	I_D	70	A
Drain Current (Pulse) PW≤10μs, duty cycle≤1%	I_{DP}	280	A
Power Dissipation Tc=25°C	P_D	2.1	W
		72	
Junction Temperature	Tj	175	°C
Storage Temperature	Tstg	−55 to +175	°C
Source Current (Body Diode)	I_S	70	A
Avalanche Energy (Single Pulse) (Note 2)	E_{AS}	82	mJ
Lead Temperature for Soldering Purposes, 3mm from Case for 10 Seconds	T_L	260	°C

Note 1 : Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2 : V_{DD}=48V, L=100μH, I_{AV}=30A (Fig.1)

Thermal Resistance Ratings

Parameter	Symbol	Value	Unit
Junction to Case Steady State	$R_{\theta JC}$	2.08	°C/W
Junction to Ambient (Note 3)	$R_{\theta JA}$	71.4	

Note 3 : Insertion mounted

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ELECTRICAL CHARACTERISTICS at Ta = 25°C (Note 4)

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=10mA, V_{GS}=0V	100			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS}(th)$	V_{DS}=10V, I_D=1mA	2		4	V
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=35A		50		S
Static Drain to Source On-State Resistance	$R_{DS}(on)1$	I_D=35A, V_{GS}=15V		9.0	10.8	mΩ
	$R_{DS}(on)2$	I_D=35A, V_{GS}=10V		9.8	12.8	mΩ
Input Capacitance	Ciss	V_{DS}=50V, f=1MHz		2,010		pF
Output Capacitance	Coss			840		pF
Reverse Transfer Capacitance	Crss			21		pF
Turn-ON Delay Time	$t_d(on)$	See Fig.2		30		ns
Rise Time	t_r			180		ns
Turn-OFF Delay Time	$t_d(off)$			55		ns
Fall Time	t_f			40		ns
Total Gate Charge	Qg	V_{DS}=48V, V_{GS}=10V, I_D=70A		26		nC
Gate to Source Charge	Qgs			9		nC
Gate to Drain “Miller” Charge	Qgd			8		nC
Forward Diode Voltage	V_{SD}	I_S=70A, V_{GS}=0V		1.1	1.5	V
Reverse Recovery Time	t_{rr}	See Fig.3 I_S=70A, V_{GS}=0V, di/dt=100A/μs		95		ns
Reverse Recovery Charge	Q_{rr}			240		nC

Note 4 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Fig.1 Unclamped Inductive Switching Test Circuit

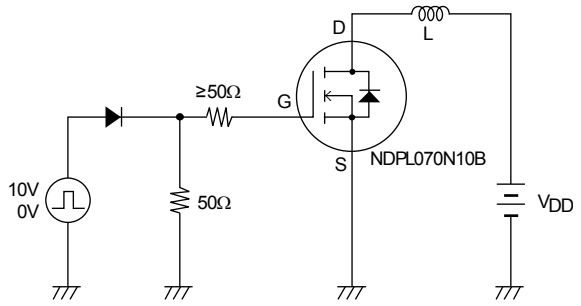


Fig.2 Switching Time Test Circuit

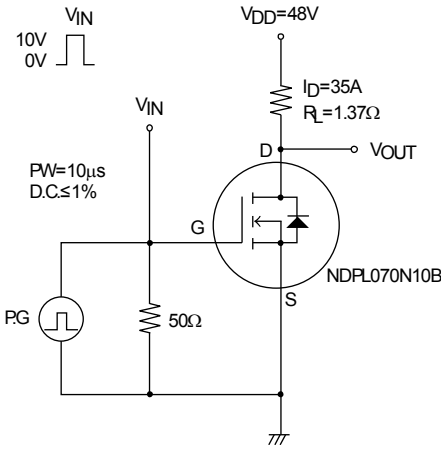
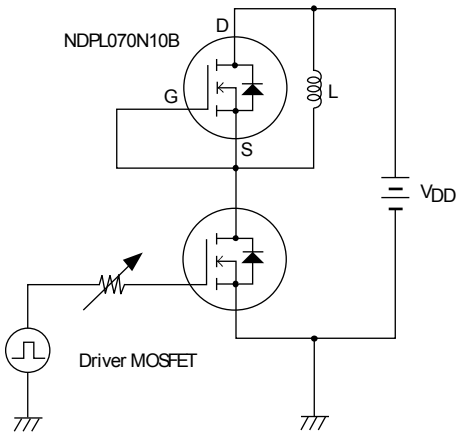
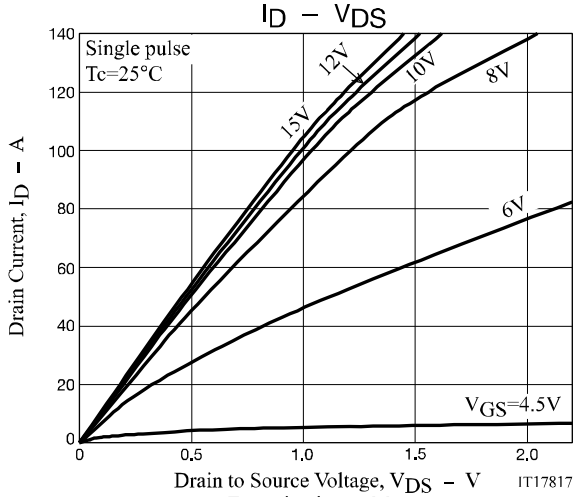
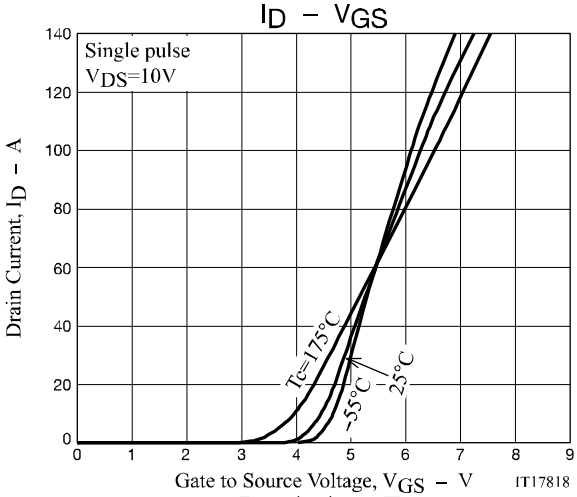
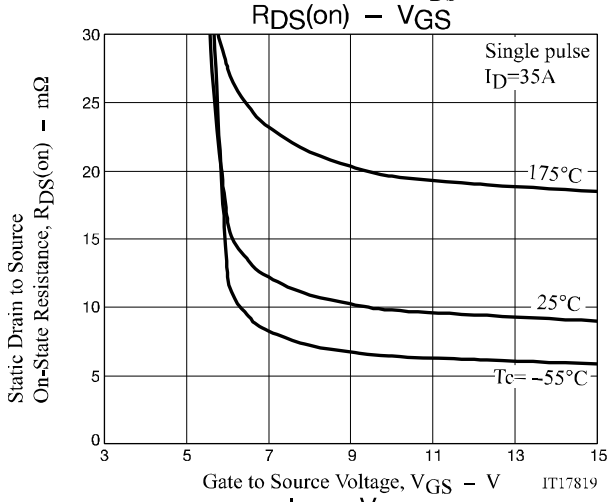


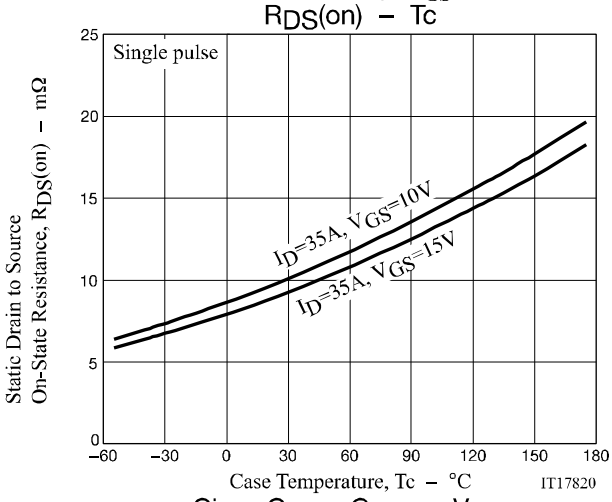
Fig.3 Reverse Recovery Time Test Circuit

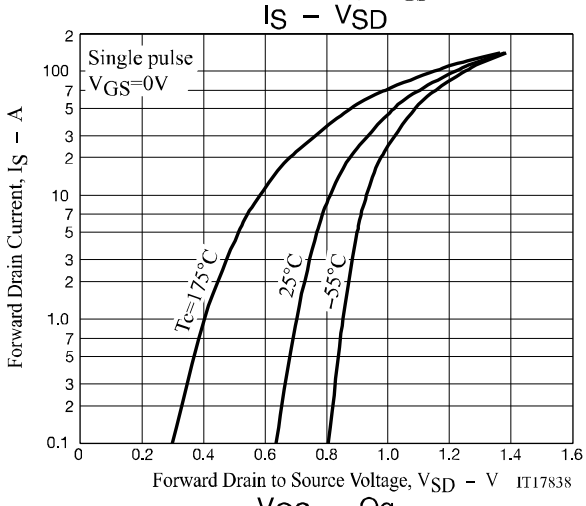


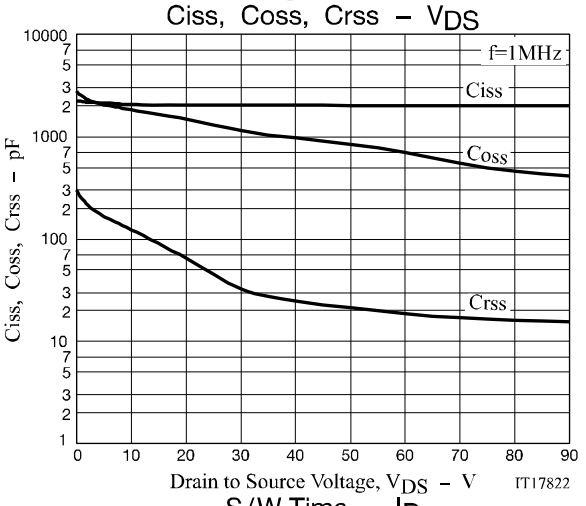

ID – VDS
Single pulse
Tc=25°C
12V
10V
8V
15V
6V
VGS=4.5V
Drain Current, ID – A
Drain to Source Voltage, VDS – V
IT17817

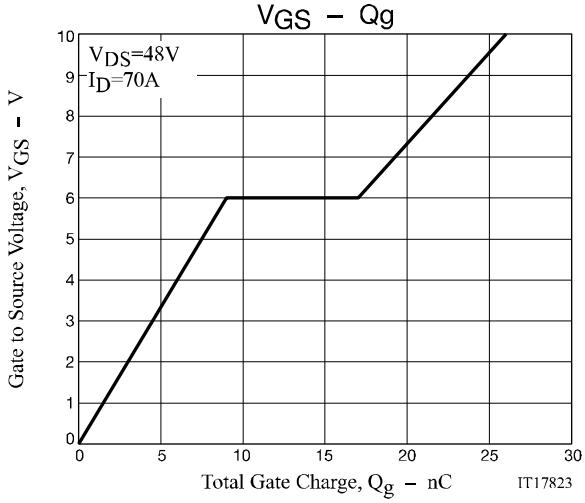

ID – VGS
Single pulse
VDS=10V
Tc=175°C
–55°C
25°C
Drain Current, ID – A
Gate to Source Voltage, VGS – V
IT17818

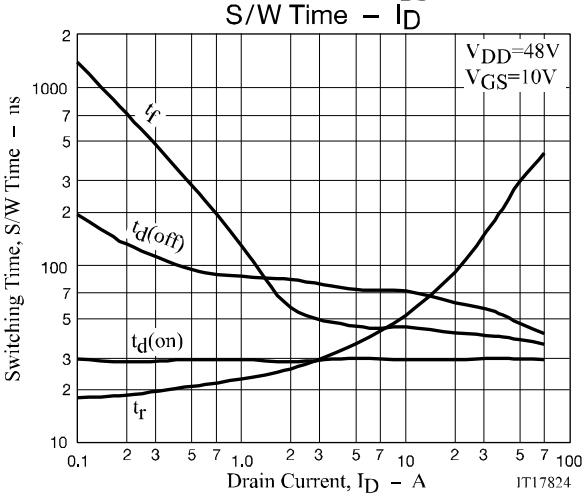

RDS(on) – VGS
Single pulse
ID=35A
175°C
25°C
Tc= –55°C
Static Drain to Source
On-State Resistance, RDS(on) – mΩ
Gate to Source Voltage, VGS – V
IT17819

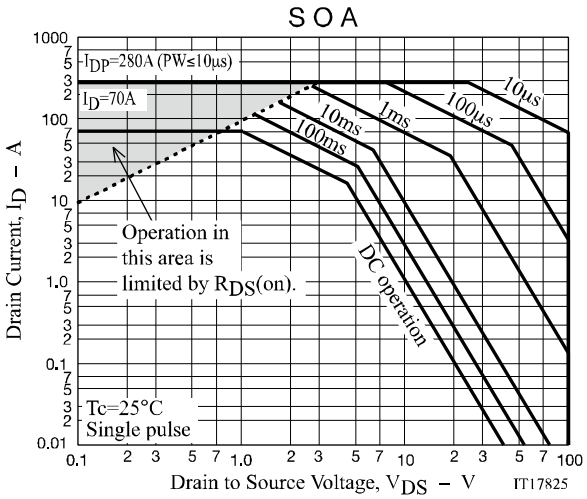

RDS(on) – Tc
Single pulse
ID=35A, VGS=10V
ID=35A, VGS=15V
Static Drain to Source
On-State Resistance, RDS(on) – mΩ
Case Temperature, Tc – °C
IT17820

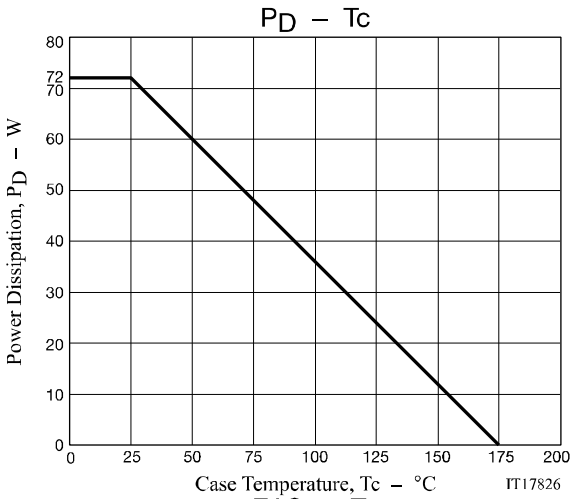

IS – VSD
Single pulse
VGS=0V
Tc=175°C
25°C
–55°C
Forward Drain Current, IS – A
Forward Drain to Source Voltage, VSD – V
IT17838

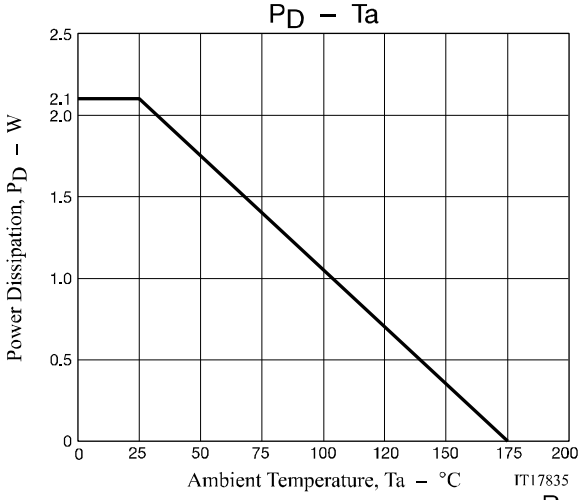

Ciss, Coss, Crss – VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain to Source Voltage, VDS – V
IT17822

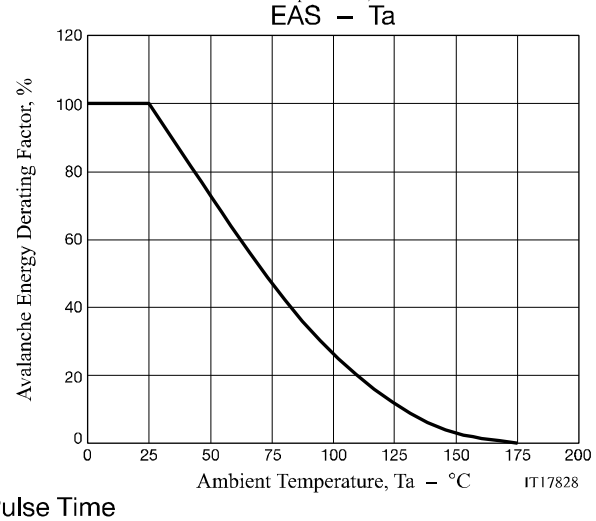

VGS – Qg
VDS=48V
ID=70A
Gate to Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT17823

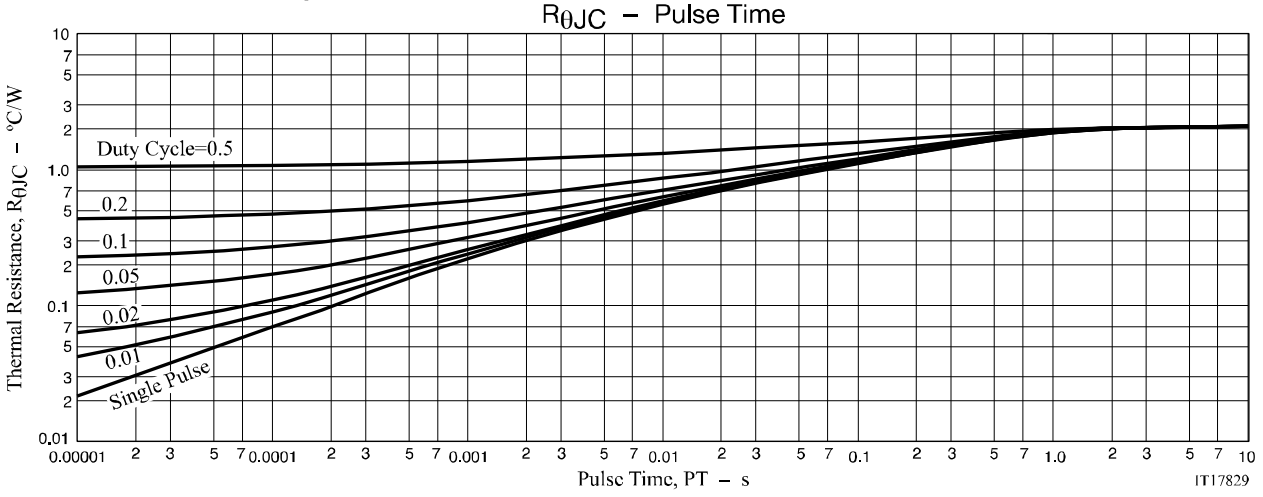

S/W Time – ID
VDD=48V
VGS=10V
tf
td(off)
td(on)
tr
Switching Time, S/W Time – ns
Drain Current, ID – A
IT17824


S O A
IDP=280A (PW≤10μs)
ID=70A
10μs
100μs
1ms
10ms
100ms
DC operation
Operation in
this area is
limited by RDS(on).
Tc=25°C
Single pulse
Drain Current, ID – A
Drain to Source Voltage, VDS – V
IT17825


PD – Tc
Power Dissipation, PD – W
Case Temperature, Tc – °C
IT17826


PD – Ta
Power Dissipation, PD – W
Ambient Temperature, Ta – °C
IT17835

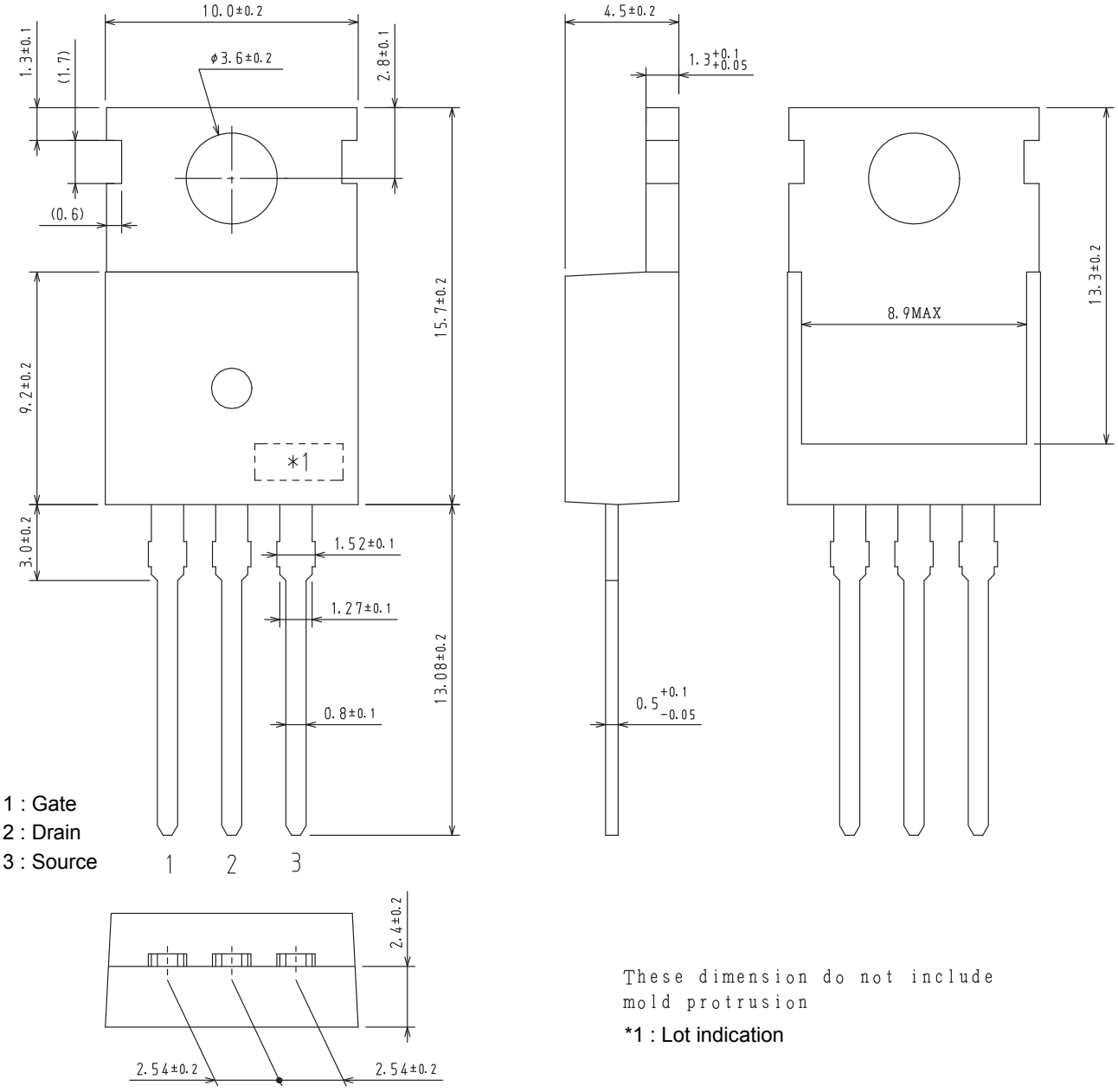

EAS – Ta
Avalanche Energy Derating Factor, %
Ambient Temperature, Ta – °C
IT17828


RθJC – Pulse Time
Duty Cycle=0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Thermal Resistance, RθJC – °C/W
Pulse Time, PT – s
IT17829

PACKAGE DIMENSIONS

unit : mm

TO-220, 3-Lead / TO-220-3L
CASE 221AU
ISSUE O



These dimension do not include mold protrusion

*1 : Lot indication

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)
NDPL070N10BG	070N10	TO-220, 3-Lead / TO-220-3L (Pb-Free)	50 / Tube

Note on usage : Since the NDPL070N10B is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.