# 1:6 Low Jitter Universal Buffer/Level Translator with 2:1 Input Mux

## Features

- 6 differential or 12 LVCMOS outputs
- Ultra-low additive jitter: 100 fs rms
- Wide frequency range: 1 to 725 MHz
- Any-format input with pin selectable output formats: LVPECL, Low Power LVPECL, LVDS, CML, HCSL, LVCMOS
- 2:1 mux with hot-swappable inputs
- Glitchless input clock switching
- Synchronous output enable
- Output clock division: /1, /2, /4
- Low output-output skew: <50 ps
- Low propagation delay variation: <400 ps
- Independent $V_{DD}$ and $V_{DDO}$ : 1.8/2.5/3.3 V
- Excellent power supply noise rejection (PSRR)
- Selectable LVCMOS drive strength to tailor jitter and EMI performance
- Small size: 32-QFN (5 mm x 5 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: –40 to +85 °C

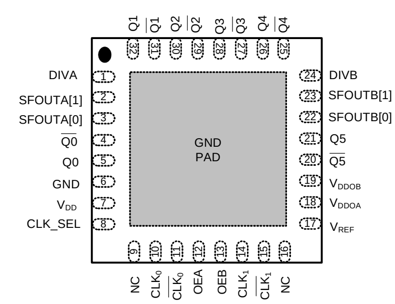

**Ordering Information:**
See page 24.

## Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

**Pin Assignments**

**Si53301**

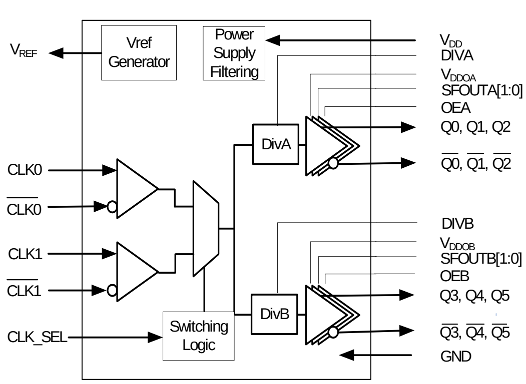



Patents pending

## Description

The Si53301 is an ultra low jitter six output differential buffer with pin-selectable output clock signal format and divider selection. The Si53301 features a 2:1 mux with glitchless switching, making it ideal for redundant clocking applications. The Si53301 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from 1 to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53301 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

## Functional Block Diagram



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# 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Ambient Operating Temperature | $T_A$ | | –40 | — | 85 | °C |
| Supply Voltage Range* | $V_{DD}$ | LVDS, CML, HCSL, LVCMOS | 1.71 | 1.8 | 1.89 | V |
| | | LVPECL, low power LVPECL, LVDS, CML, HCSL, LVCMOS | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| Output Buffer Supply Voltage* | $V_{DDO}$ | LVDS, CML, HCSL, LVCMOS | 1.71 | — | 1.89 | V |
| | | LVPECL, low power LVPECL, LVDS, CML, HCSL, LVCMOS | 2.38 | — | 2.63 | V |
| | | | 2.97 | — | 3.63 | V |

***Note:** Core supply $V_{DD}$ and output buffer supplies $V_{DDO}$ are independent.

**Table 2. Input Clock Specifications**

($V_{DD}$=1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$=–40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential Input Common Mode Voltage | $V_{CM}$ | $V_{DD}$ = 2.5 V± 5%, 3.3 V± 10% | 0.05 | — | — | V |
| Input Swing (single-ended, peak-to-peak) | $V_{IN}$ | | 0.1 | — | 1.1 | V |
| Input Voltage High | $V_{IH}$ | | $V_{DD}$ x 0.7 | — | — | V |
| Input Voltage Low | $V_{IL}$ | | — | — | $V_{DD}$ x 0.3 | V |
| Input Capacitance | $C_{IN}$ | | — | 5 | — | pF |

**Table 3. DC Common Characteristics**
($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | | — | TBD | 100 | mA |
| Output Buffer Supply Current (Per Clock Output) @100 MHz | $I_{DDOX}$ | LVPECL (3.3 V) | — | 35 | — | mA |
| | | Low Power LVPECL (3.3 V) | — | 30 | — | mA |
| | | LVDS (3.3 V) | — | 20 | — | mA |
| | | CML (3.3 V) | — | 30 | — | mA |
| | | HCSL, 100 MHz, 2 pF load (3.3 V) | — | 35 | — | mA |
| | | CMOS (1.8 V, SFOUT = Open/0), per output, $C_L$ = 5 pF, 200 MHz | — | 5 | — | mA |
| | | CMOS (2.5 V, SFOUT = Open/0), per output, $C_L$ = 5 pF, 200 MHz | — | 8 | — | mA |
| | | CMOS (3.3 V, SFOUT = 0/1), per output, $C_L$ = 5 pF, 200 MHz | — | 15 | — | mA |
| Leakage Current | $I_L$ | Input leakage at all inputs except CLKIN, $V_{IN}$ = 0 V | — | — | TBD | µA |
| | | Input leakage at CLKIN $V_{IN}$ = 0 V | — | — | TBD | µA |
| Voltage Reference | $V_{REF}$ | $V_{REF}$ pin | — | VDD/2 | — | V |
| Input High Voltage | $V_{IH}$ | SFOUTX, DIVX 3-level input pins | 0.85 x VDD | — | — | V |
| Input Mid Voltage | $V_{IM}$ | SFOUTX, DIVX 3-level input pins | 0.45 x VDD | 0.5 x VDD | 0.55 x VDD | V |
| Input Low Voltage | $V_{IL}$ | SFOUTX, DIVXpin 3-level input pins | — | — | 0.15 x VDD | V |
| Internal Pull-down Resistor | $R_{DOWN}$ | CLK_SEL, DIVA, DIVB, SFOUTA[1], SFOUTB[1] | — | 25 | — | kΩ |
| Internal Pull-up Resistor | $R_{UP}$ | SFOUTA[1], SFOUTB[1], DIVA, DIVB, OEA, OEB | — | 25 | — | kΩ |

**Table 4. DC Characteristics—LVPECL and Low Power LVPECL**
($V_{DD}$ = 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage High | $V_{OH}$ | $R_L$ = 50 Ω to $V_{DDOX}$ – 2 V | $V_{DDOX}$ – 1.145 | — | $V_{DDOX}$ – 0.895 | V |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 50 Ω to $V_{DDOX}$ – 2 V | $V_{DDOX}$ – 1.945 | — | $V_{DDOX}$ – 1.695 | V |
| Output DC Common Mode Voltage | $V_{COM}$ | | $V_{DDOX}$ – 1.895 | — | $V_{DDOX}$ – 1.425 | V |
| Single-Ended Output Swing | $V_{SE}$ | Terminate unused outputs to $R_L$ = 50 Ω to $V_{DDOX}$ – 2 V | 0.25 | 0.60 | 0.85 | V |

**Table 5. DC Characteristics—CML**
($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single-Ended Output Swing | $V_{SE}$ | Terminated as shown in Figure 8 (CML termination). | 300 | 400 | 500 | mV |

**Table 6. DC Characteristics—LVDS**
($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single-Ended Output Swing | $V_{SE}$ | $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 247 | — | 454 | mV |
| Output Common Mode Voltage ($V_{DDO}$ = 2.5 V or 3.3V) | $V_{COM1}$ | $V_{DDOX}$ = 2.38 to 2.63 V, 2.97 to 3.63 V, $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 1.10 | 1.25 | 1.35 | V |
| Output Common Mode Voltage ($V_{DDO}$ = 1.8 V) | $V_{COM2}$ | $V_{DDOX}$ = 1.71 to 1.89 V, $R_L$ = 100 Ω across $Q_N$ and $\overline{Q}_N$ | 0.85 | 0.97 | 1.10 | V |

### Table 7. DC Characteristics—LVCMOS

($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage High* | $V_{OH}$ | | 0.85 x $V_{DDOX}$ | — | — | V |
| Output Voltage Low* | $V_{OL}$ | | — | — | 0.15 x $V_{DDOX}$ | V |
| ***Note:** $I_{OH}$ and $I_{OL}$ per the Output Signal Format Table for specific $V_{DDOX}$ and SFOUTX settings. | | | | | | |

### Table 8. DC Characteristics—HCSL

($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage High | $V_{OH}$ | $R_L$ = 50 Ω to GND | 550 | 700 | 850 | mV |
| Output Voltage Low | $V_{OL}$ | $R_L$ = 50 Ω to GND | –150 | 0 | 150 | mV |
| Single-Ended Output Swing | $V_{SE}$ | $R_L$ = 50 Ω to GND | — | 700 | — | mV |
| Crossing Voltage | $V_C$ | $R_L$ = 50 Ω to GND | 250 | 350 | 550 | mV |

### Table 9. AC Characteristics

($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Frequency | F | LVPECL, low power LVPECL, LVDS, CML, HCSL | 1 | — | 725 | MHz |
| | | LVCMOS | 1 | — | 200 | MHz |
| Duty Cycle **Note:** 50% input duty cycle. | $D_C$ | 200 MHz, 50 Ω to $V_{DD}$/2, 20/80% $T_R$/$T_F$<10% of period (LVCMOS) | TBD | TBD | TBD | % |
| | | 20/80% $T_R$/$T_F$<10% of period (Differential) | 48 | 50 | 52 | % |
| Minimum Input Clock Slew Rate[1] | SR | Required to meet prop delay and additive jitter specifications (20–80%) | 0.75 | — | — | V/ns |

**Notes:**

1. For clock division applications, a minimum input clock slew rate of 30 mV/ns is required.
2. See Figure 4.
3. Defined as skew between outputs on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to $V_{DDOX}$ (1.8 V = 50 $mV_{PP}$, 2.5/3.3 V = 100 $mV_{PP}$) and noise spur amplitude measured. See AN491 for further details.

**Table 9. AC Characteristics (Continued)**
($V_{DD}$ = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, $T_A$ = –40 to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise/Fall Time | $T_R/T_F$ | LVPECL, LVDS, CML, HCSL, 20/80% | | | 350 | ps |
| | | 200 MHz, 50 Ω, 20/80%, 2 pF load (LVCMOS) | TBD | TBD | 750 | ps |
| Minimum Input Pulse Width | $T_W$ | | 500 | — | — | ps |
| Additive Jitter (Differential Clock Input) | J | $V_{DD}$ = 2.5/3.3 V, LVPECL/LVDS, F = 725 MHz, 0.75 V/ns input slew rate | — | 60 | 80 | fs |
| Propagation Delay | $T_{PLH}$, $T_{PHL}$ | Low to high, high to low Single-ended | TBD | — | TBD | ns |
| | | Low to high, high to low Differential | TBD | — | TBD | ns |
| Output Enable Time[2] | $T_{EN}$ | F = 1 MHz | — | 2 | — | µs |
| | | F = 100 MHz | — | 60 | — | ns |
| | | F = 725 MHz | — | 50 | — | ns |
| Output Disable Time[2] | $T_{DIS}$ | F = 1 MHz | — | 2 | — | µs |
| | | F = 100 MHz | — | 25 | — | ns |
| | | F = 725 MHz | — | 15 | — | ns |
| Output to Output Skew | $T_{SK}$ | Identical Configuration, Single-ended ($Q_N$ to $Q_M$) | — | — | 100 | ps |
| | | Identical Configuration, Differential ($Q_N$ to $Q_M$) | — | — | 50 | ps |
| Part to Part Skew[3] | $T_{PS}$ | Identical configuration | — | 50 | — | ps |
| Power Supply Noise Rejection[4] | PSRR | 10 kHz sinusoidal noise | — | –90 | — | dBc |
| | | 100 kHz sinusoidal noise | — | –90 | — | dBc |
| | | 500 kHz sinusoidal noise | — | –80 | — | dBc |
| | | 1 MHz sinusoidal noise | — | –70 | — | dBc |

**Notes:**
1. For clock division applications, a minimum input clock slew rate of 30 mV/ns is required.
2. See Figure 4.
3. Defined as skew between outputs on different devices operating at the same supply voltages, temperatures, and equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to $V_{DDOX}$ (1.8 V = 50 $mV_{PP}$, 2.5/3.3 V = 100 $mV_{PP}$) and noise spur amplitude measured. See AN491 for further details.

## Table 10. Thermal Conditions

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $\theta_{JA}$ | Still air | 49.6 | °C/W |
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | Still air | 32.3 | °C/W |

## Table 11. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Storage Temperature | $T_S$ | | –55 | — | 150 | °C |
| Supply Voltage | $V_{DD}$ | | –0.5 | — | 3.8 | V |
| Input Voltage | $V_{IN}$ | | –0.5 | — | $V_{DD}$+ 0.3 | V |
| Output Voltage | $V_{OUT}$ | | — | — | $V_{DD}$+ 0.3 | V |
| ESD Sensitivity | HBM | HBM, 100 pF, 1.5 kΩ | 2000 | — | — | V |
| ESD Sensitivity | CDM | | 500 | — | — | V |
| Peak Soldering Reflow Temperature | $T_{PEAK}$ | Pb-Free; Solder reflow profile per JEDEC J-STD-020 | — | — | 260 | °C |
| Maximum Junction Temperature | $T_J$ | | — | — | 125 | °C |

**Note:** Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

# 2. Functional Description

The Si53301 is a low jitter, low skew 1:6 differential buffer with an integrated 2:1 input mux. The device has a universal input that accepts most common differential or LVCMOS input signals. A clock select pin is used to select the active input clock. The selected clock input is routed to two independent banks of outputs. Each output bank features control pins to select signal format, output enable, output divider setting and LVCMOS drive strength.

## 2.1. Universal, Any-Format Input

The Si53301 has a universal input stage that enables simple interfacing to a wide variety of clock formats, including LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 12 and 13 summarize the various ac- and dc-coupling options supported by the device. Figures 3 and 4 show the recommended input clock termination options.

**Table 12. LVPECL, LVCMOS, and LVDS**

| | LVPECL | | LVCMOS | | LVDS | |
|---|---|---|---|---|---|---|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | N/A | N/A | No | Yes | Yes | No |
| 2.5/3.3 V | Yes | Yes | No | Yes | Yes | Yes |

**Table 13. HCSL and CML**

| | HCSL | | CML | |
|---|---|---|---|---|
| | AC-Couple | DC-Couple | AC-Couple | DC-Couple |
| 1.8 V | No | No | Yes | No |
| 2.5/3.3 V | No | Yes (3.3 V) | Yes | No |

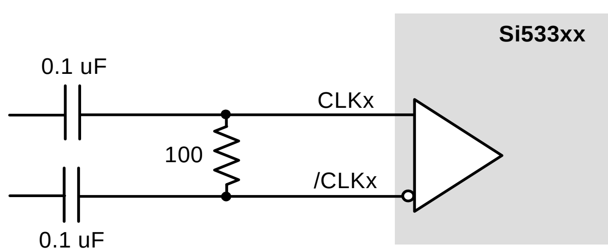



**Figure 1. Differential LVPECL, LVDS, CML AC-Coupled Input Termination**

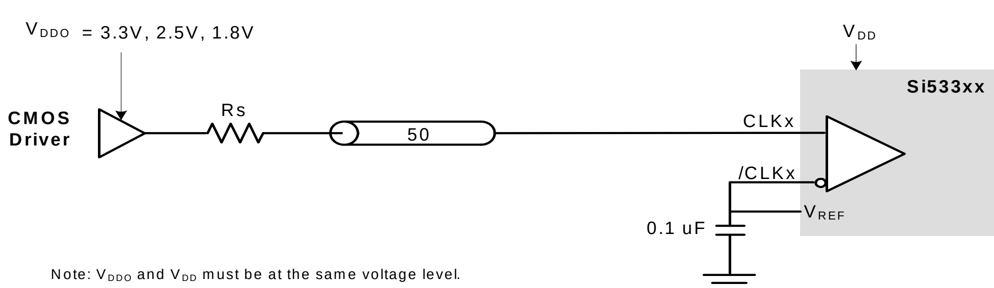
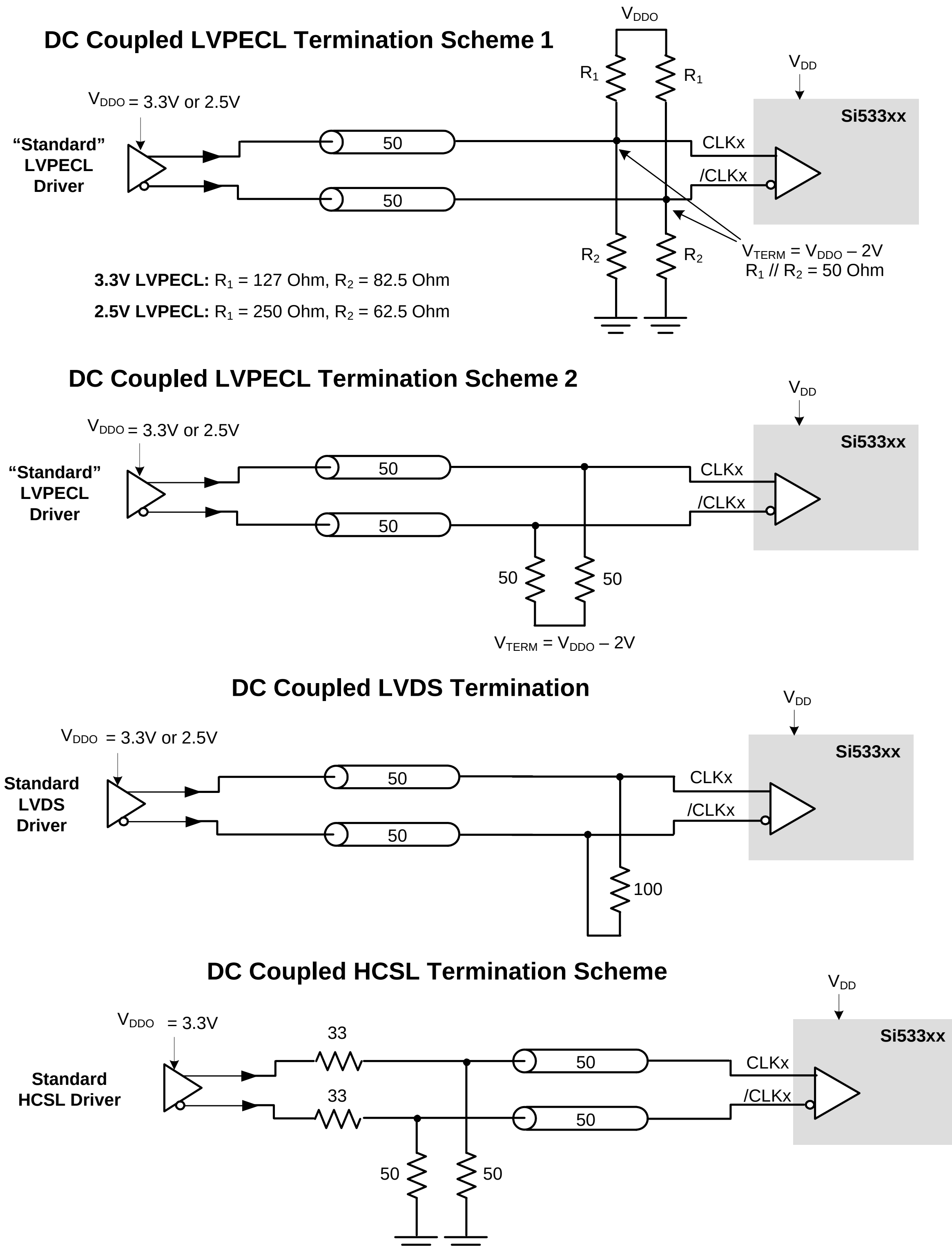



**Figure 2. LVCMOS DC-Coupled Input Termination**




Note: 33 Ohm series termination is optional depending on the location of the receiver.

**Figure 3. Differential DC-Coupled Input Terminations**

## 2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to $V_{DD}$. The inverting input is biased with a 75 kΩ pullup to $V_{DD}$.

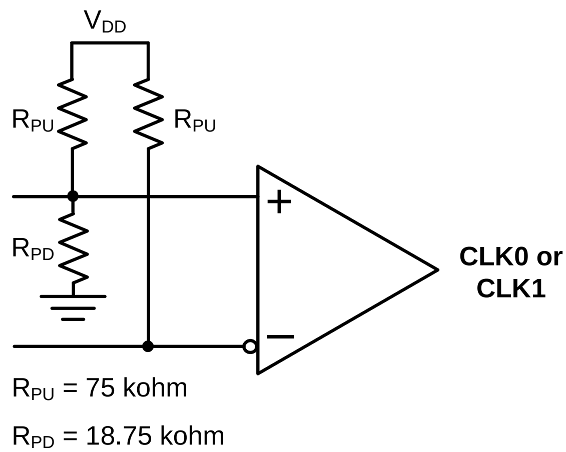



**Figure 4. Input Bias Resistors**

## 2.3. Universal, Any-Format Output Buffer

The Si53301 has highly flexible output drivers that support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUTA[1:0] and SFOUTB[1:0] are 3-level inputs that can be pin-strapped to select the Bank A and Bank B clock signal formats, respectively. This feature enables the device to be used for format translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each $V_{DDO}$ setting.

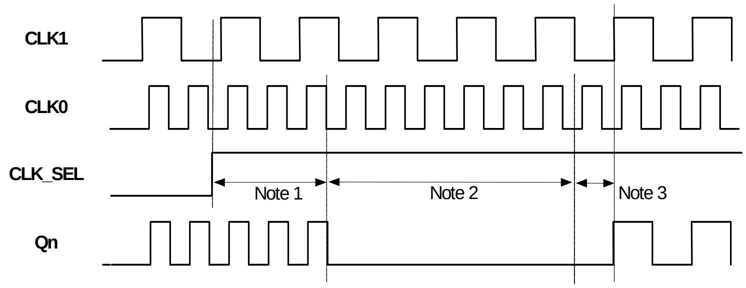
**Table 14. Output Signal Format Selection**

| SFOUTX[1] | SFOUTX[0] | $V_{DDOX}$ = 3.3 V | $V_{DDOX}$ = 2.5 V | $V_{DDOX}$ = 1.8 V |
|---|---|---|---|---|
| Open* | Open* | LVPECL | LVPECL | N/A |
| 0 | 0 | LVDS | LVDS | LVDS |
| 0 | 1 | LVCMOS, 24 mA drive | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive |
| 1 | 0 | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive |
| 1 | 1 | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive | LVCMOS, 6 mA drive |
| Open* | 0 | LVCMOS, 6 mA drive | LVCMOS, 4 mA drive | LVCMOS, 2 mA drive |
| Open* | 1 | LVPECL Low power | LVPECL Low power | N/A |
| 0 | Open* | CML | CML | CML |
| 1 | Open* | HCSL | HCSL | HCSL |

***Note:** SFOUTX are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin floats to $V_{DD}/2$.

## 2.4. Glitchless Clock Input Switching

The Si53301 features glitchless switching between two valid input clocks. Figure 5 illustrates that switching between input clocks does not generate runt pulses or glitches at the output.




Notes:

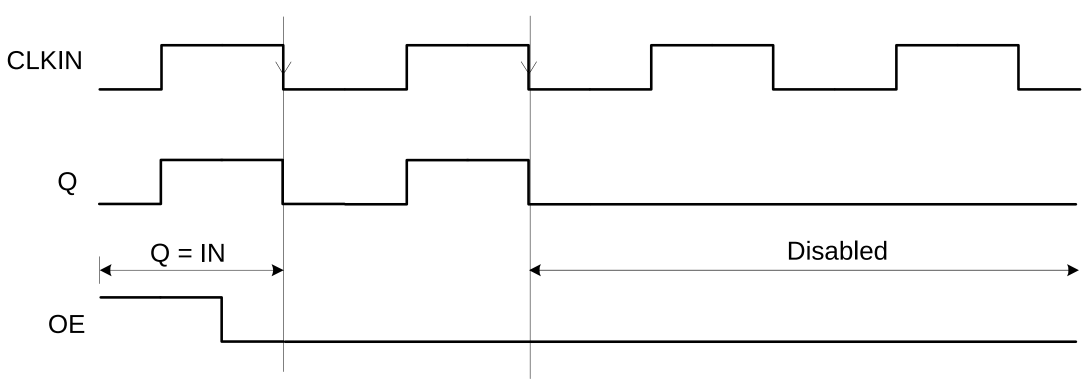
1. $Q_n$ continues with CLK0 for 2-3 falling edges of CLK0.
2. $Q_n$ is disabled low for 2-3 falling edges of CLK1 .
3. $Q_n$ starts on the first rising edge after 1 + 2.

**Figure 5. Glitchless Input Clock Switch**

The Si53301 supports glitchless switching between clocks at the same frequency. In addition, the device supports glitchless switching between 2 input clocks that are up to 10x different in frequency. When a switchover to a new clock is made, the output will disable low after two or three clock cycles of the previously-selected input clock. The outputs will remain low for up to three clock cycles of the newly-selected clock, after which the outputs will start from the newly-selected input. In the case a switchover to an absent clock is made, the output will glitchlessly stop low and wait for edges of the newly selected clock. A switchover from an absent clock to a live clock will also be glitchless. Note that the CLK_SEL input should not be toggled faster than 1/250th the frequency of the slower input clock.

## 2.5. Synchronous Output Enable

The Si53301 features a synchronous output enable (disable) feature. Output enable is sampled and synchronized on the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.




Note 1. Outputs are disabled after 1 to 2 negative edges of the input clock.

**Figure 6. Synchronous Output Enable**

When OE is low, Q is held low and $\overline{Q}$ is held high for differential output formats. For LVCMOS output format options, both Q and $\overline{Q}$ are held low when OE is set low. The device outputs are enabled when the output enable pin is unconnected.

## 2.6. Flexible Output Divider

The Si53301 provides optional clock division in addition to clock distribution. The divider setting for each bank of output clocks is selected via 3-level control pins as shown in the table below. Leaving the DIVX pins open will force a divider value of 1 which is the default mode of operation.

**Table 15. Post Divider Selection**

| DIVX | Divider Value |
|---|---|
| Open* | ÷1 (default) |
| 0 | ÷2 |
| 1 | ÷4 |

***Note:** DIVX are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin floats to VDD/2.

## 2.7. Input Mux and Output Enable Logic

The Si53301 provides two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The table below summarizes the input and output clock based on the input mux and output enable pin settings.

**Table 16. Input Mux and Output Enable Logic**

| CLK_SEL | CLK0 | CLK1 | OE[1] | Q[2] |
|---|---|---|---|---|
| L | L | X | H | L |
| L | H | X | H | H |
| H | X | L | H | L |
| H | X | H | H | H |
| X | X | X | L | L[3] |

**Notes:**
1. Output enable active high
2. On the next negative transition of CLK0 or CLK1.
3. Single-end: Q = low, $\overline{Q}$ = high
   Differential: Q = low, $\overline{Q}$ = high

## 2.8. Power Supply ($V_{DD}$ and $V_{DDOX}$)

The device includes separate core ($V_{DD}$) and output driver supplies ($V_{DDOX}$). This feature allows the core to operate at a lower voltage than $V_{DDO}$, reducing current consumption in mixed supply applications. The core $V_{DD}$ supports 3.3 V, 2.5 V, or 1.8 V. Each output bank has its own $V_{DDOX}$ supply, supporting 3.3 V, 2.5 V, or 1.8 V.

## 2.9. Output Clock Termination Options

The recommended output clock termination options are shown below. Unused output clocks should be left floating.

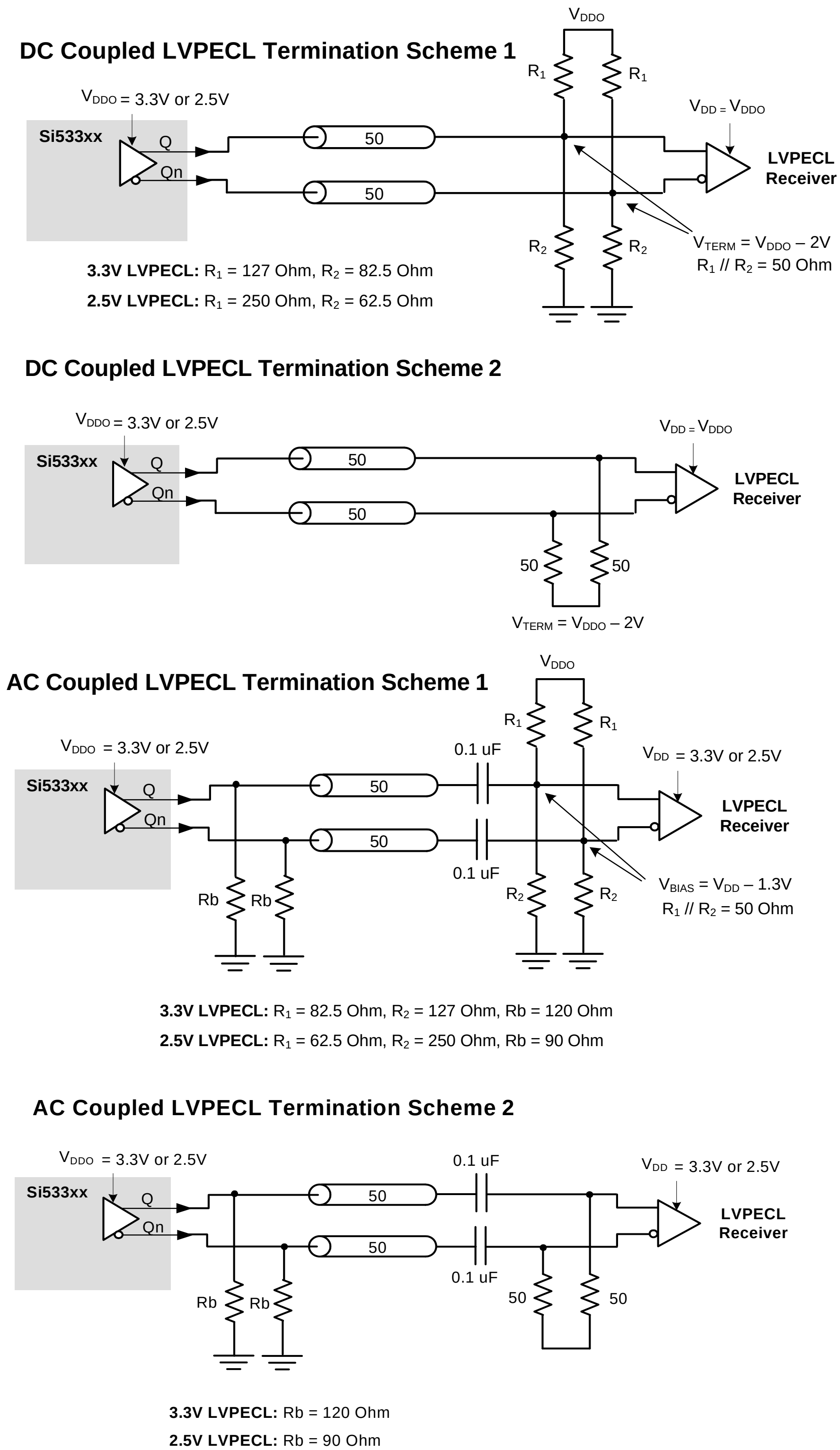



**Figure 7. LVPECL Output Termination**

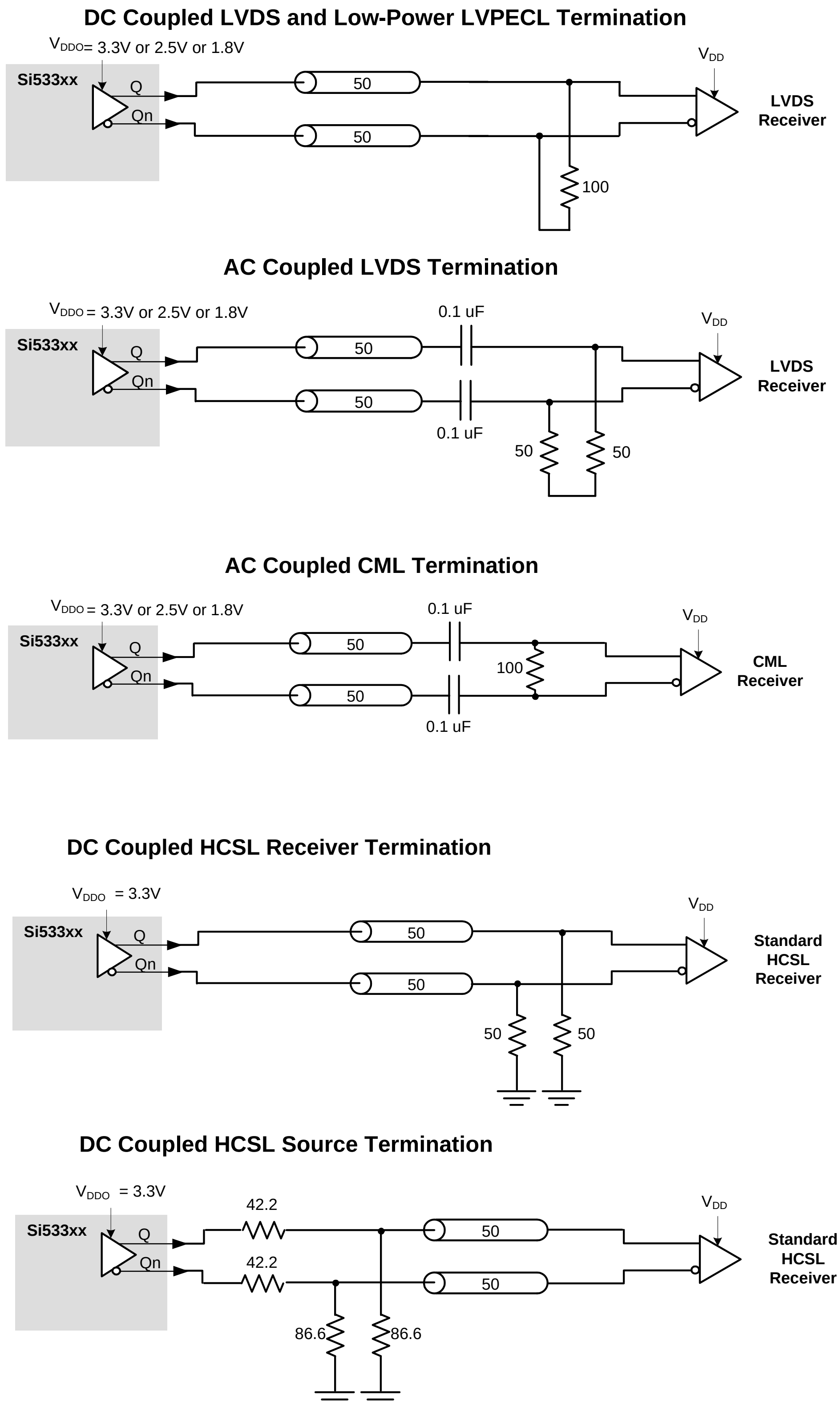



**Figure 8. LVDS, CML, and HCSL Output Termination**

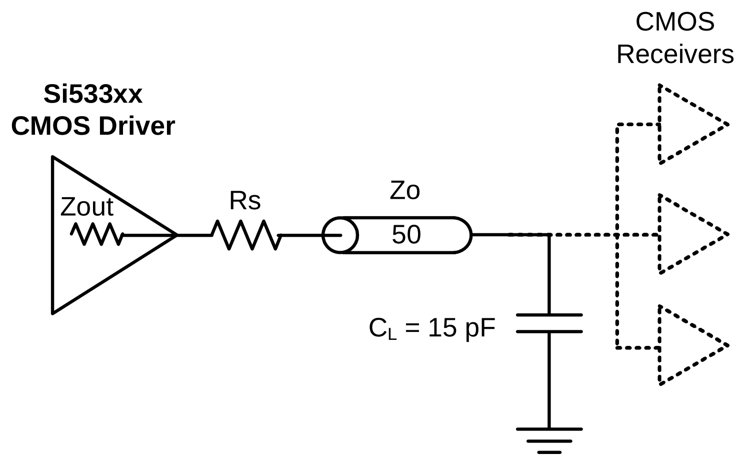



**Figure 9. LVCMOS Output Termination**

**Table 17. Recommended LVCMOS $R_S$ Series Termination**

| SFOUTX[1] | SFOUTX[0] | $R_S$ (ohms) | | |
|---|---|---|---|---|
| | | 3.3 V | 2.5 V | 1.8 V |
| 0 | 1 | 33 | 33 | 33 |
| 1 | 0 | 33 | 33 | 33 |
| 1 | 1 | 0 | 0 | 0 |
| Open | 0 | 0 | 0 | 0 |

## 2.10. AC Timing Waveforms

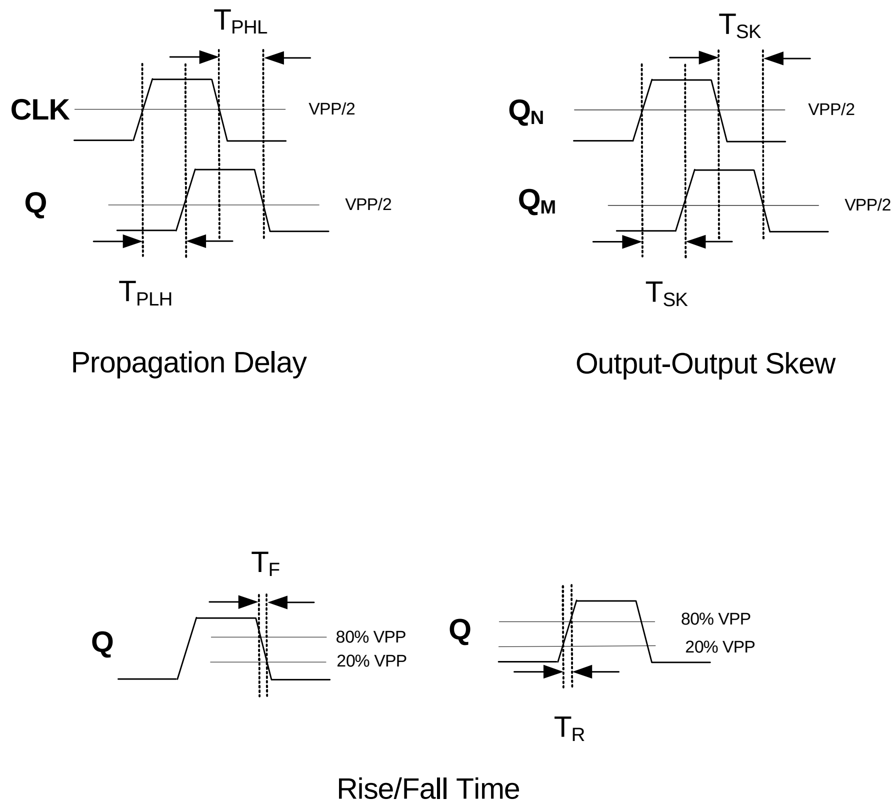
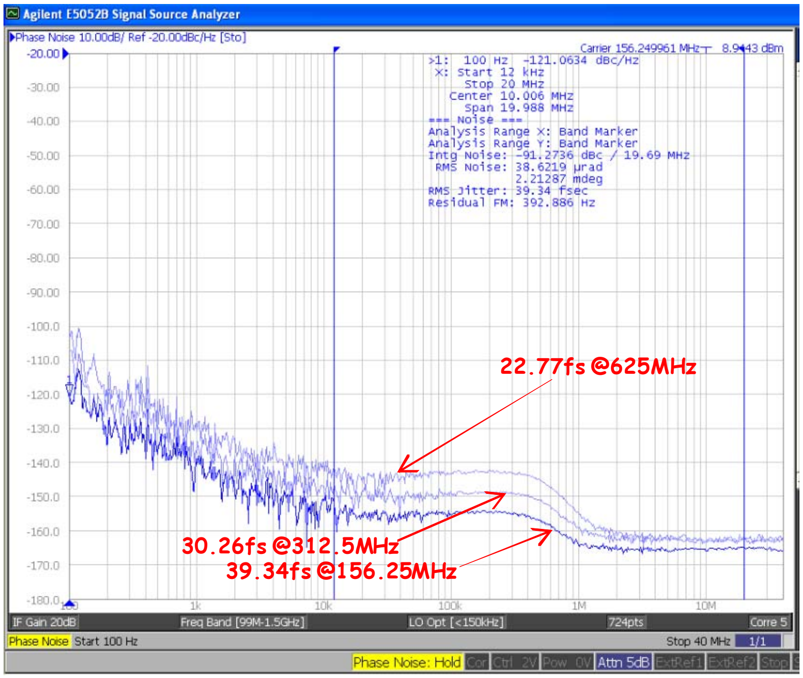
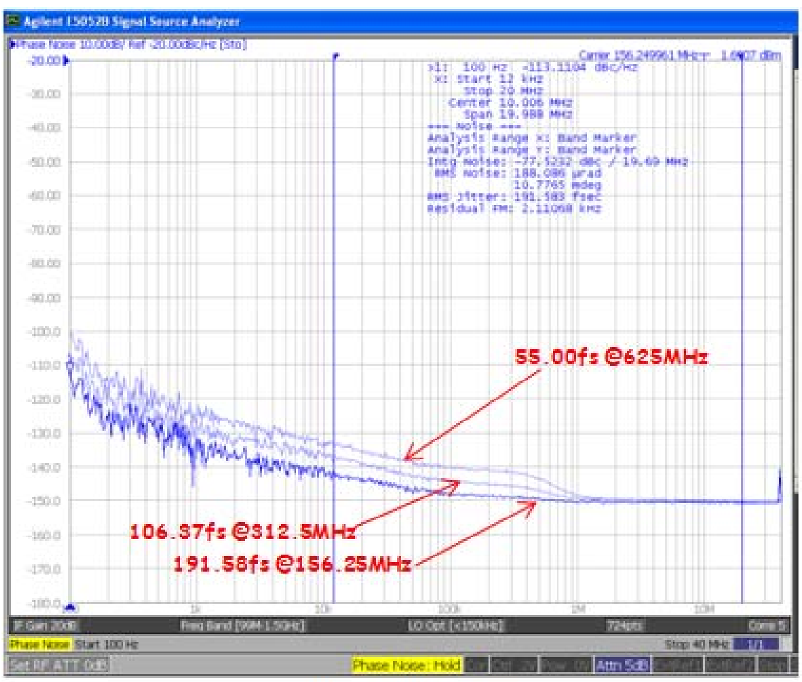



**Figure 10. AC Waveforms**

## 2.11. Typical Phase Noise Performance




Source Jitter




Total Jitter

**Figure 11. Si53301 Phase Noise**

**Note:** Measured single-endedly.

**Table 18. Si53301 Additive Jitter**

| Frequency (MHz) | Source Jitter (fs) | Total Jitter (fs) | Additive Jitter (fs) |
|---|---|---|---|
| 156.25 | 39.34 | 191.58 | 187.50 |
| 312.5 | 30.26 | 106.37 | 101.98 |
| 625 | 22.77 | 55.00 | 50.07 |

## 2.12. Input Mux Noise Isolation

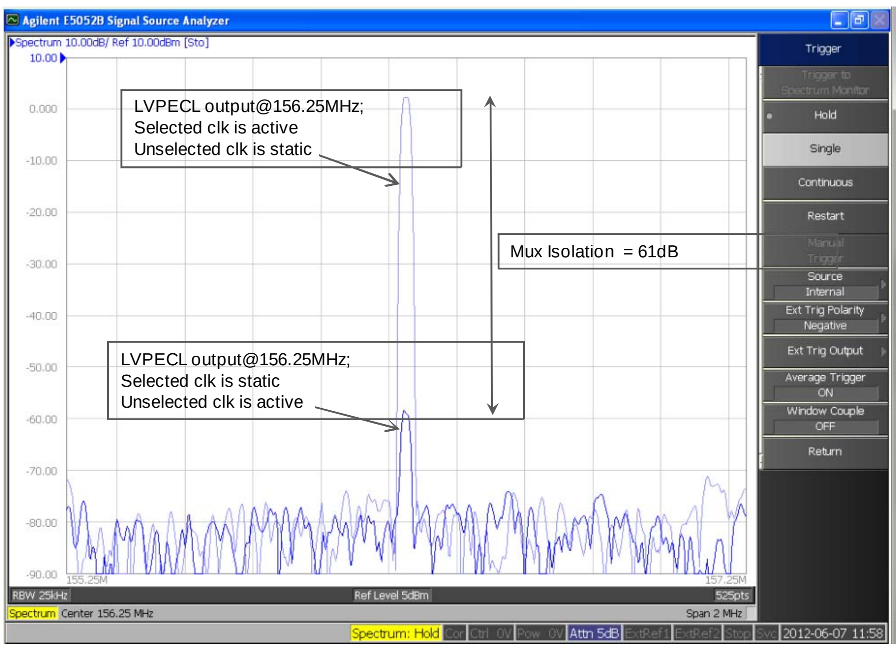



**Figure 12. Input Mux Noise Isolation**

## 2.13. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see “AN491: Power Supply Rejection for Low Jitter Clocks”.

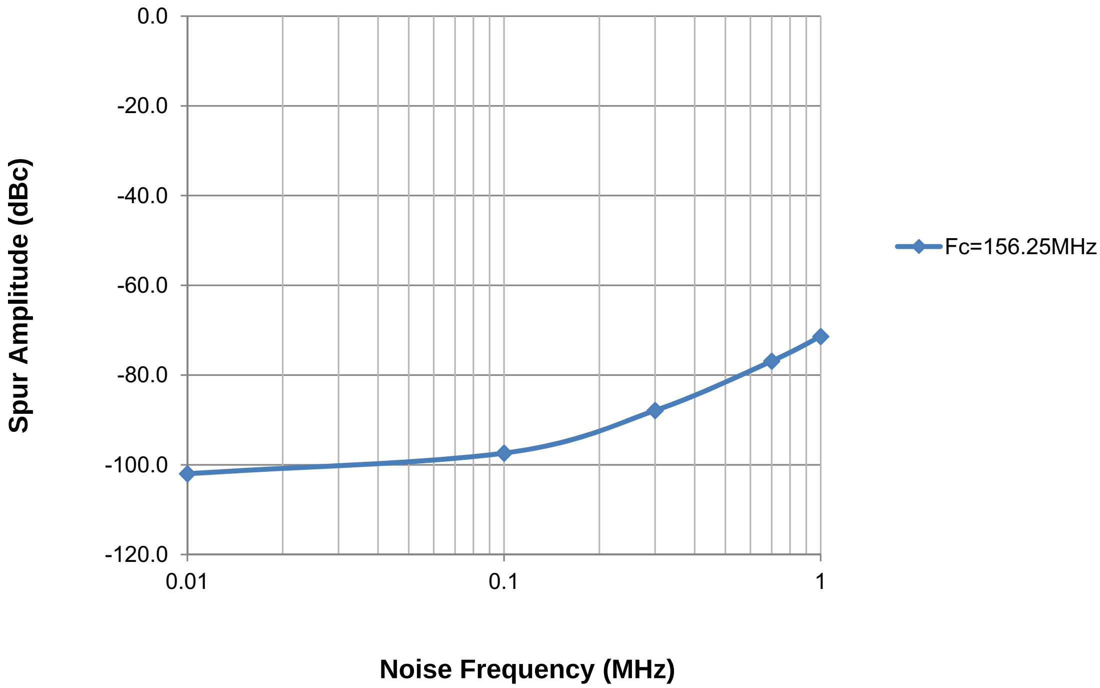



**Figure 13. Power Supply Noise Rejection (100 mVpp Sinusoidal Power Supply Noise Applied)**

# 3. Pin Description: 32-Pin QFN

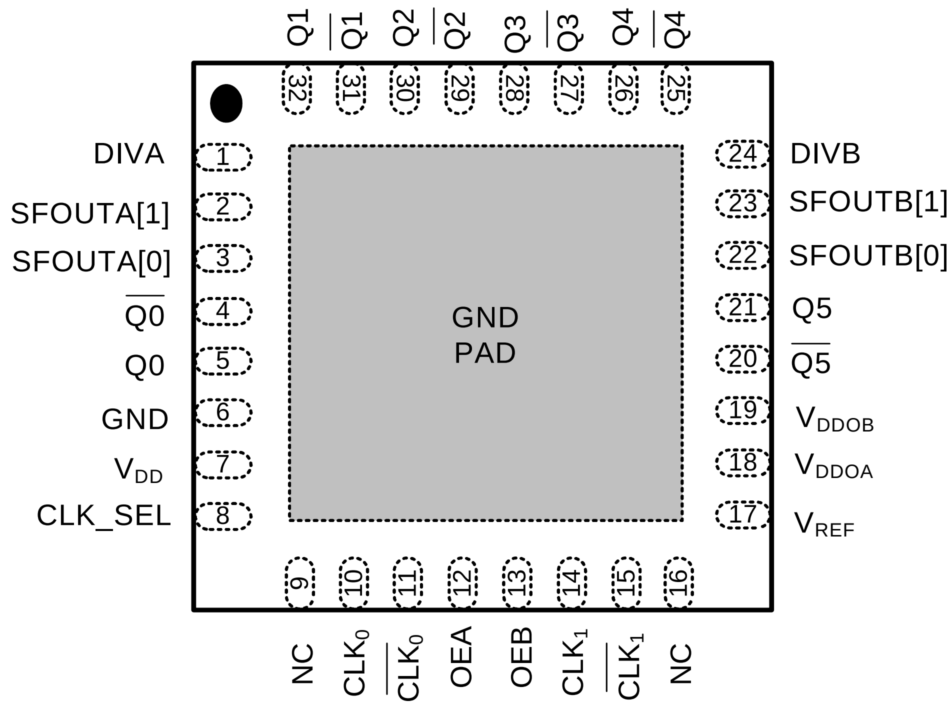



**Table 19. Pin Description**

| Pin | Name | Description |
|---|---|---|
| 1 | DIVA | Output divider control pin for Bank A<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 2 | SFOUTA[1] | Output signal format control pin for Bank A<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 3 | SFOUTA[0] | Output signal format control pin for Bank A<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 4 | $\overline{Q0}$ | Output clock 0 (complement) |
| 5 | Q0 | Output clock 0 |
| 6 | GND | Ground |
| 7 | $V_{DD}$ | Core voltage supply.<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DD}$ pin as possible. |

**Table 19. Pin Description (Continued)**

| Pin | Name | Description |
|---|---|---|
| 8 | CLK_SEL | Mux input select pin (LVCMOS)<br>Clock inputs are switched without the introduction of glitches.<br>When CLK_SEL is high, CLK1 is selected.<br>When CLK_SEL is low, CLK0 is selected.<br>CLK_SEL contains an internal pull-down resistor. |
| 9 | NC | No connect. |
| 10 | CLK0 | Input clock 0 |
| 11 | $\overline{\text{CLK0}}$ | Input clock 0 (complement)<br>When the CLK0 is driven by a single-end input, connect $V_{REF}$ to $\overline{\text{CLK0}}$.<br>$\overline{\text{CLK0}}$ contains an internal pull-up resistor. |
| 12 | OEA | Output enable—Bank A<br>When OE=high, the Bank A outputs are enabled.<br>When OE=low, Q is held low, and $\overline{\text{Q}}$ is held high for differential formats.<br>For LVCMOS, both Q and $\overline{\text{Q}}$ are held low when OE is set low.<br>OEA contains an internal pull-up resistor. |
| 13 | OEB | Output enable—Bank B<br>When OE=high, the Bank B outputs are enabled.<br>When OE=low, Q is held low, and $\overline{\text{Q}}$ is held high for differential formats.<br>For LVCMOS, both Q and $\overline{\text{Q}}$ are held low when OE is set low.<br>OEB contains an internal pull-up resistor. |
| 14 | CLK1 | Input clock 1 |
| 15 | $\overline{\text{CLK1}}$ | Input clock 1 (complement)<br>When the CLK1 is driven by a single-end input, connect $V_{REF}$ to $\overline{\text{CLK1}}$.<br>$\overline{\text{CLK1}}$ contains an internal pull-up resistor. |
| 16 | NC | No connect. |
| 17 | $V_{REF}$ | Input reference voltage<br>When driven by a LVCMOS clock input, connect the unused clock input to $V_{REF}$ and a 0.1 µF cap to ground. When driven by a differential clock, do not connect the $V_{REF}$ pin. |
| 18 | $V_{DDOA}$ | Output voltage supply—Bank A (Outputs: Q0 to Q2)<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DDOA}$ pin as possible. |
| 19 | $V_{DDOB}$ | Output voltage supply—Bank B (Outputs: Q3 to Q5)<br>Bypass with 1.0 µF capacitor and place as close to the $V_{DDOB}$ pin as possible. |
| 20 | $\overline{\text{Q5}}$ | Output clock 5 (complement) |
| 21 | Q5 | Output clock 5 |

**Table 19. Pin Description (Continued)**

| Pin | Name | Description |
|---|---|---|
| 22 | SFOUTB[0] | Output signal format control pin for Bank B.<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 23 | SFOUTB[1] | Output signal format control pin for Bank B.<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 24 | DIVB | Output divider configuration bit for Bank B.<br>Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or $V_{DD}$. |
| 25 | $\overline{Q4}$ | Output clock 4 (complement) |
| 26 | Q4 | Output clock 4 |
| 27 | $\overline{Q3}$ | Output clock 3 (complement) |
| 28 | Q3 | Output clock 3 |
| 29 | $\overline{Q2}$ | Output clock 2 (complement) |
| 30 | Q2 | Output clock 2 |
| 31 | $\overline{Q1}$ | Output clock 1 (complement) |
| 32 | Q1 | Output clock 1 |
| GND Pad | GND | Ground Pad.<br>Power supply ground and thermal relief. |

## 4. Ordering Guide

| Part Number | Package | PB-Free, ROHS-6 | Temperature |
|---|---|---|---|
| Si53301-B-GM | 32-QFN | Yes | –40 to 85 °C |

# 5. Package Outline

## 5.1. 5x5 mm 32-QFN Package Diagram

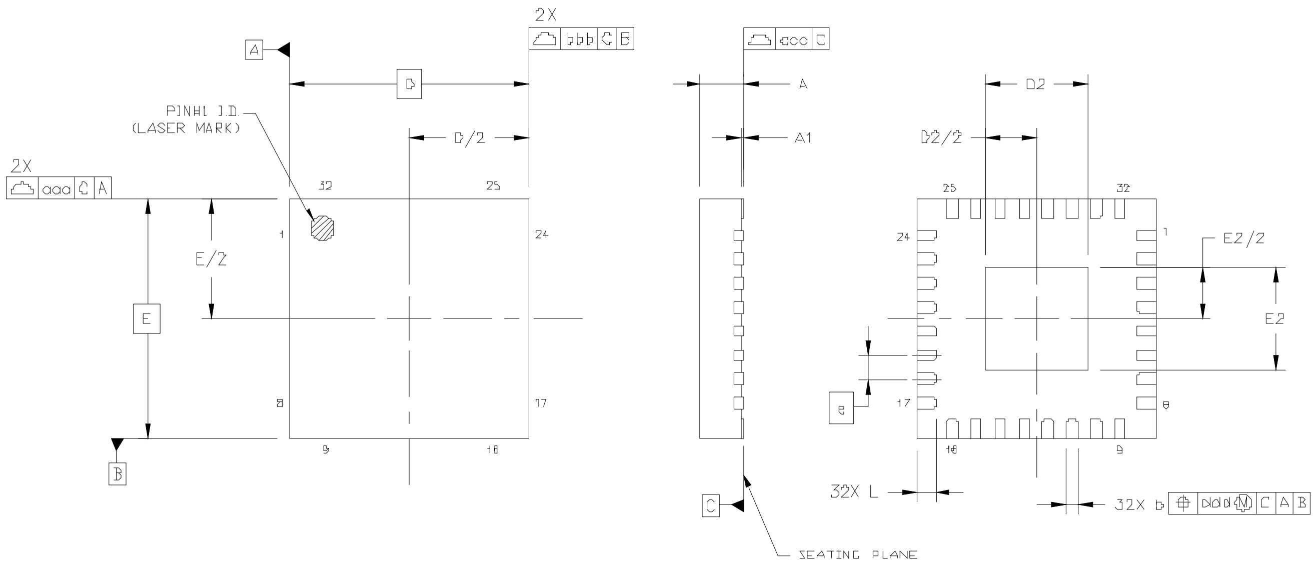



**Figure 14. Si53301 5x5 mm 32-QFN Package Diagram**

**Table 20. Package Dimensions**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.20 | 0.25 | 0.30 |
| D | | 5.00 BSC | |
| D2 | 2.00 | 2.15 | 2.30 |
| e | | 0.50 BSC | |
| E | | 5.00 BSC | |
| E2 | 2.00 | 2.15 | 2.30 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.08 | |
| ddd | | 0.10 | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.

# 6. PCB Land Pattern

## 6.1. 5x5 mm 32-QFN Package Land Pattern

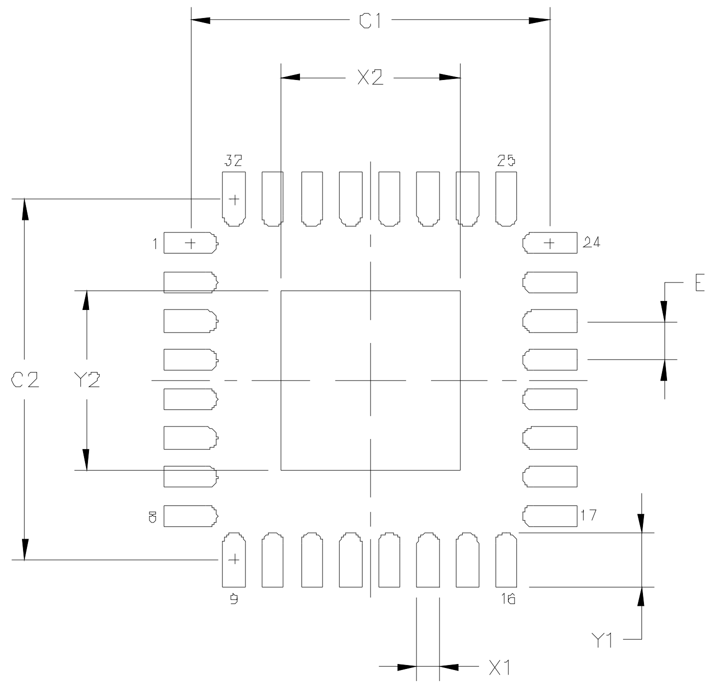



**Figure 15. Si53301 5x5 mm 32-QFN Package Land Pattern**

**Table 21. PCB Land Pattern**

| Dimension | Min | Max | Dimension | Min | Max |
|---|---|---|---|---|---|
| C1 | 4.52 | 4.62 | X2 | 2.20 | 2.30 |
| C2 | 4.52 | 4.62 | Y1 | 0.59 | 0.69 |
| E | 0.50 BSC | | Y2 | 2.20 | 2.30 |
| X1 | 0.20 | 0.30 | | | |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 $\mu$m minimum, all the way around the pad.

**Stencil Design**

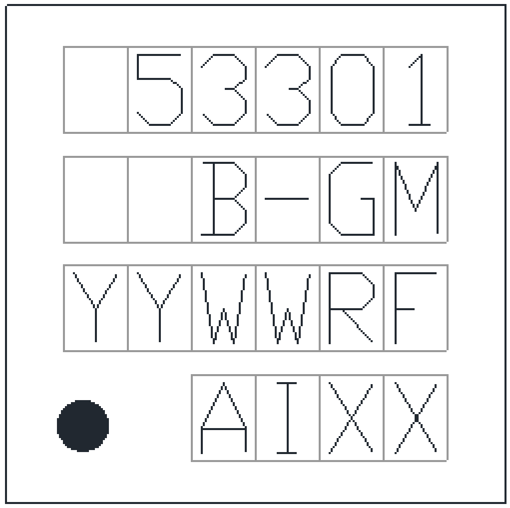
1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 7. Top Marking

## 7.1. Si53301 Top Marking




## 7.2. Top Marking Explanation

| | | |
|---|---|---|
| **Mark Method:** | Laser | |
| **Font Size:** | 2.0 Point (28 mils)<br>Center-Justified | |
| **Line 1 Marking:** | Device Part Number | **53301** |
| **Line 2 Marking:** | Device Revision/Type | **B-GM** |
| **Line 3 Marking:** | YY = Year<br>WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| | R = Die Rev<br>F = Wafer Fab | First two characters of the Manufacturing Code from the Assembly Purchase Order form. |
| **Line 4 Marking** | Circle = 0.5 mm Diameter<br>Lower-Left Justified | Pin 1 Identifier |
| | A = Assembly Site<br>I = Internal Code<br>XX = Serial Lot Number | Last four characters of the Manufacturing Code from the Assembly Purchase Order form. |

# Document Change List

## Revision 0.1 to Revision 0.2

- Removed LOS.

## Revision 0.2 to Revision 0.3

- Formatting changes.
- Updated part number to revision B.
- Added phase noise plot, PSRR figure, input mux isolation figure.
- Updated AC/DC specifications.

## Revision 0.3 to Revision 0.31

- Formatting changes.

## Revision 0.31 to Revision 0.4

- Updated part number to revision B.
- Added phase noise plot, PSRR figure, input mux isolation figure.
- Updated AC/DC specifications.

## NOTES:

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