NB7VPQ16M

1.8V/2.5V CML 12.5 Gbps Programmable Pre−Emphasis Copper/Cable Driver with Selectable Equalizer Receiver

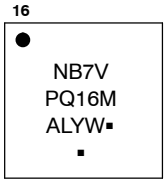
Multi−Level Inputs w/ Internal Termination

ON Semiconductor®

http://onsemi.com

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

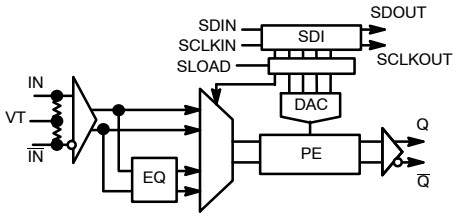


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

Description

The NB7VPQ16M is a high performance single channel programmable Pre−Emphasis CML Driver with a selectable Equalizer Receiver that operates up to 14 Gbps typical with a 1.8 V or 2.5 V power supply. When placed in series with a Data/Clock path, the NB7VPQ16M inputs will compensate the degraded signal transmitted across a FR4 PCB backplane or cable interconnect. Therefore, the serial data rate is increased by reducing Inter−Symbol Interference (ISI) caused by losses in copper interconnect or long cables.

The Pre−Emphasis buffer is controlled using a serial bus via the Serial Data In (SDIN) and Serial Clock In (SCLKIN) control inputs and contains circuitry which provides sixteen programmable Pre−Emphasis settings to select the optimal output compensation level.

These selectable output levels will handle various backplane lengths and cable lines. The first four SDIN bits (D3:D0) will digitally select 0 dB through 12 dB typical of de−emphasis (see Table 1).

For cascaded applications, the shifted SDIN and SCLKIN signals are presented at the SDOUT and SCLKOUT pins.

The 5th−bit (LSB) of the serial data bits allows for enabling the equalization function of the receiver.

The differential Data / Clock inputs incorporate a pair of internal 50 Ω termination resistors, in a 100 Ω center−tapped configuration, via the VT pin and will accept LVPECL, CML or LVDS logic levels. This feature provides transmission line termination on−chip, at the receiver end, eliminating external components.

The NB7VPQ16M is a member of the GigaComm™ Family of high performance Data/Clock products with Pre−Emphasis/Equalization (PEEQ).

Features

- Maximum Input Data Rate > 12.5 Gbps
- Maximum Input Clock Frequency > 8 GHz
- Drives Up To 18−inches of FR4
- (16) Programmable Output De−emphasis Levels; 0 dB through 12 dB
- 200 ps Typical Propagation Delay
- Differential CML Outputs, 400 mV Peak−to−Peak, Typical (PE = 0 dB)
- Operating Range: V_{CC} = 1.71 V to 2.625 V, GND = 0 V
- Internal Output Termination Resistors, 50 Ω
- QFN−16 Package, 3 mm x 3 mm
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices

July, 2009 − Rev. 0
Publication Order Number:
NB7VPQ16M/D

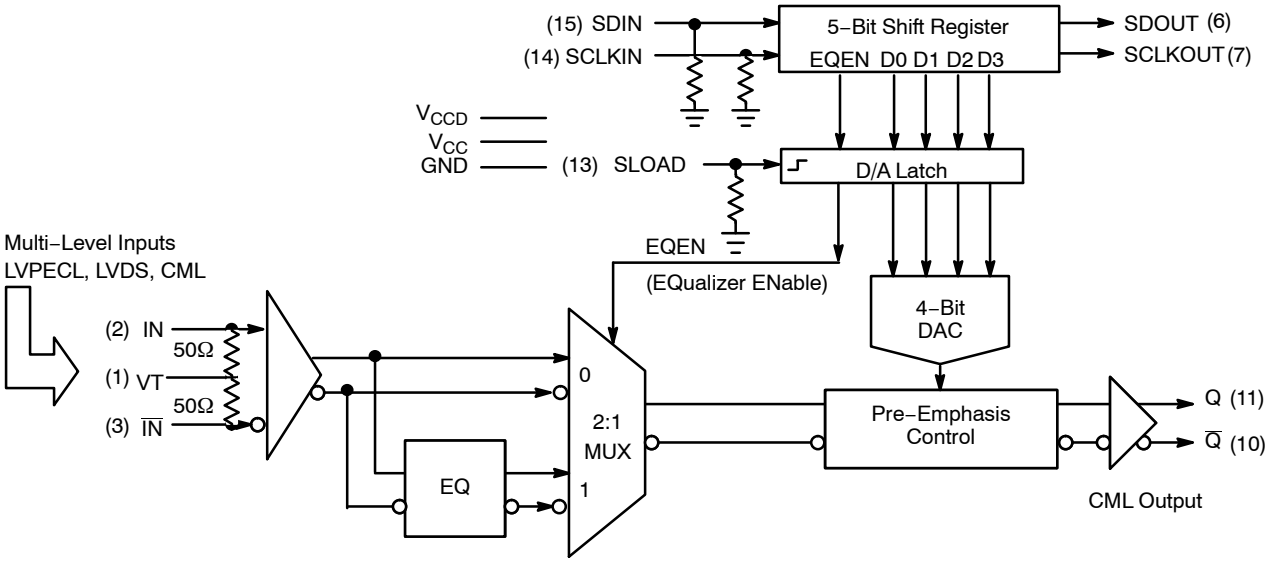
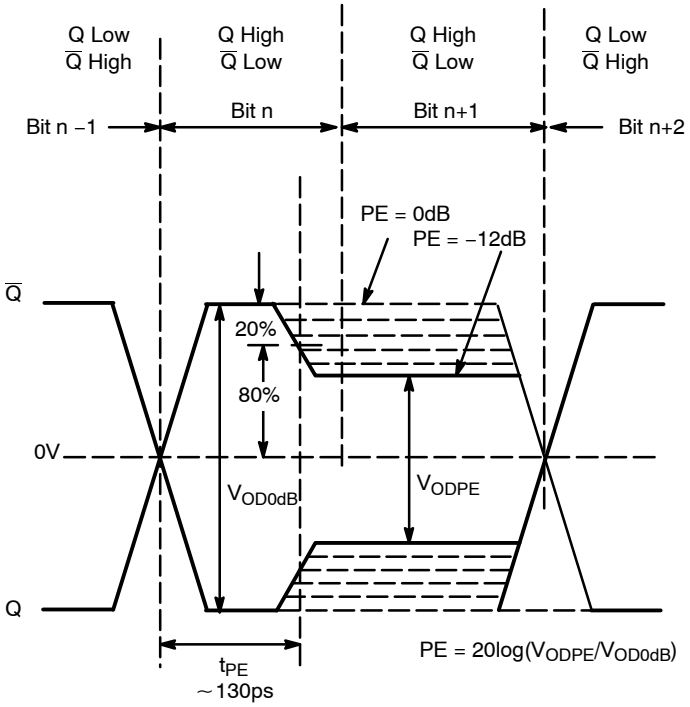


Figure 2. Detailed Block Diagram of NB7VPQ16M



V_{OD0dB} − Differential Output Voltage without Pre−Emphasis
V_{ODPE} − Differential Output Voltage with Pre−Emphasis

Figure 3. Illustration of Output Waveform Definition

Table 1. TYPICAL PRE−EMPHASIS CONTROL TABLE, EQ = 0, 25°C, V_{CC} = 1.8 V

Decimal	4−bit PE MSB D3	D2	D1	LSB D0	PE Output Compensation in dB Approximate @ 1 GHz	V_{ODPE} Typ (mV)
00	0	0	0	0	0 dB (Default)	435
01	0	0	0	1	−1.0 dB	390
02	0	0	1	0	−1.5 dB	365
03	0	0	1	1	−2.0 dB	345
04	0	1	0	0	−2.5 dB	325
05	0	1	0	1	−3.0 dB	310
06	0	1	1	0	−3.5 dB	290
07	0	1	1	1	−4.0 dB	275
08	1	0	0	0	−4.5 dB	260
09	1	0	0	1	−5.0 dB	245
10	1	0	1	0	−6.0 dB	220
11	1	0	1	1	−7.0 dB	195
12	1	1	0	0	−8.0 dB	175
13	1	1	0	1	−9.0 dB	155
14	1	1	1	0	−10.0 dB	135
15	1	1	1	1	−12.0 dB	110

Table 2. EQUALIZER ENABLE FUNCTION

EQEN	Function
0	IN/$\overline{IN}$ Inputs By−pass the Equalizer section
1	Inputs flow through the Equalizer

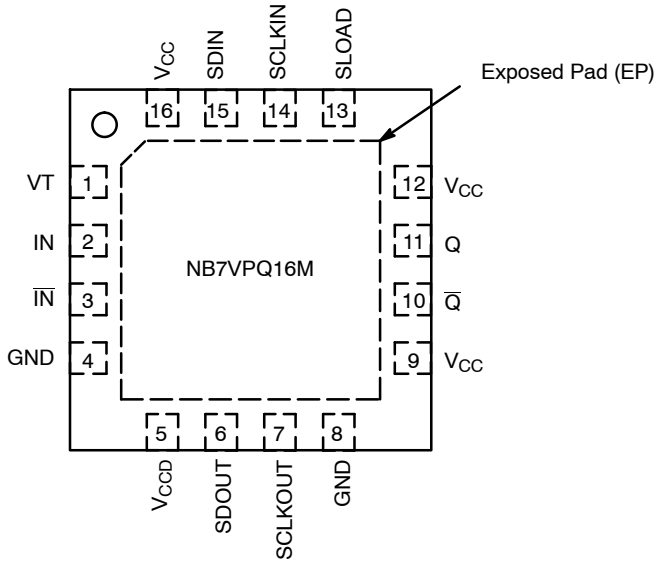


Figure 4. Pin Configuration (Top View)

Table 3. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VT		Internal 50−Ω Termination Pin for IN and $\overline{IN}$
2	IN	LVPECL, CML, LVDS Input	Non−inverted Differential Clock/Data Input. (Note 1)
3	$\overline{IN}$	LVPECL, CML, LVDS Input	Inverted Differential Clock/Data Input. (Note 1)
4	GND	−	Negative Supply Voltage; (Note 2)
5	VCCD	−	Positive Supply Voltage for Serial Bus Logic and 5−Bit DAC; (Note 2)
6	SDOUT	LVCMOS Output	Serial Data Out
7	SCLKOUT	LVCMOS Output	Serial Clock Out
8	GND	−	Negative Supply Voltage; (Note 2)
9	VCC	−	Positive Supply Voltage for the analog circuitry and CML Output buffer; (Note 2)
10	$\overline{Q}$	CML	Inverted Differential Output. (Note 1)
11	Q	CML	Non−inverted Differential Output. (Note 1)
12	VCC	−	Positive Supply Voltage for the analog circuitry and CML Output buffer; (Note 2)
13	SLOAD	LVCMOS Input	When the SLOAD pin is LOW or left open (has internal pulldown resistor), the output of the shift register will input the 4−bit DAC and set the EQEN bit. When HIGH, the input to the 4−bit DAC is locked to the state prior to when SLOAD went HIGH.
14	SCLKIN	LVCMOS Input	Serial Clock In; pin will default LOW when left open (has internal pulldown resistor)
15	SDIN	LVCMOS Input	Serial Data In; pin will default LOW when left open (has internal pulldown resistor)
16	VCC	−	Positive Supply Voltage for the analog circuitry and CML Output buffer; (Note 2)
	EP		The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is also electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pin (V_T) is connected to a common termination voltage or left open, and if no input signal is applied on IN/$\overline{IN}$ input, then the device will be susceptible to self−oscillation. Q/$\overline{Q}$ outputs have internal 50 Ω source termination resistor.
2. All V_{CC}, V_{CCD} and GND pins must be externally connected to a power supply voltage to guarantee proper device operation.

Table 4. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 4 kV > 200 V
Internal Input Pulldown Resistor		75 kΩ
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 3)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		416
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}, V_{CCD}	Positive Power Supply	GND = 0 V		3.0	V
V_{IN}	Positive Input Voltage	GND = 0 V		−0.5 to V_{CC} +0.5	V
V_{INPP}	Differential Input Voltage |IN − $\overline{IN}$|			1.89	V
I_{out}	Output Current	Continuous Surge		34 40	mA
I_{IN}	Input Current Through R_T (50 Ω Resistor)			±40	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4) TGSD 51−6 (2S2P Multilayer Test Board) with Filled Thermal Vias	0 lfpm 500 lfpm	QFN−16 QFN−16	42 35	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	QFN−16	4	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 6. DC CHARACTERISTICS POSITIVE CML OUTPUT V_{CC} = V_{CCD} = 1.71 V to 2.625 V; GND = 0 V; T_A = −40°C to 85°C (Note 5)

Symbol	Characteristic		Min	Typ	Max	Unit
POWER SUPPLY CURRENT						
I_{CC}	Power Supply Current, (Inputs and Outputs Open) PE = 0dB	V_{CC} = 2.5 V V_{CC} = 1.8 V		95 80	120 100	mA
I_{CCD}	Power Supply Current for Serial Bus and DAC (Inputs and Outputs Open)	PE = 0000 = 0dB PE = 1111 = Max		0 10	 20	mA
CML OUTPUTS PE = 0dB (Note 6, Figure 22)						
V_{OH}	Output HIGH Voltage	 V_{CC} = 2.5 V V_{CC} = 1.8 V	V_{CC} – 30 2470 1770	V_{CC} – 10 2490 1790	V_{CC} 2500 1800	mV
V_{OL}	Output LOW Voltage	V_{CC} = 2.5 V	V_{CC} – 600 1900	V_{CC} – 500 2000	V_{CC} – 400 2100	mV
		V_{CC} = 1.8 V	V_{CC} – 550 1250	V_{CC} – 450 1350	V_{CC} – 350 1450	
DATA/CLOCK INPUTS (IN, $\overline{IN}$) (Note 7) (Figure 6)						
V_{IHD}	Differential Input HIGH Voltage		1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage		GND		V_{CC} – 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})		100		1200	mV
I_{IH}	Input HIGH Current		−150	20	150	μA
I_{IL}	Input LOW Current		−150	5	150	μA
CONTROL INPUTS (SDIN, SCLKIN, SLOAD)						
V_{IH}	Input HIGH Voltage for Control Pins		V_{CCD} x 0.65		V_{CCD}	mV
V_{IL}	Input LOW Voltage for Control Pins		GND		V_{CCD} x 0.35	mV
I_{IH}	Input HIGH Current		−150	20	150	μA
I_{IL}	Input LOW Current		−150	5	150	μA
CONTROL OUTPUTS (SDOUT, SCLKOUT)						
V_{OH}	Output HIGH Voltage		V_{CC} – 200		V_{CC}	mV
V_{OL}	Output LOW Voltage		GND		200	mV
TERMINATION RESISTORS						
R_{TIN}	Internal Input Termination Resistor		45	50	55	Ω
R_{TOUT}	Internal Output Termination Resistor		45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC}.
6. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
7. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 7. AC CHARACTERISTICS V_{CC} = V_{CCD} = 1.71 V to 2.625 V; GND = 0 V; T_A = −40°C to 85°C (Note 8)

Symbol	Characteristic		Min	Typ	Max	Unit
$f_{DATAMAX}$	Maximum Input Data Rate		12.5	14		Gbps
f_{MAX}	Maximum Input Clock Frequency (Note 9)	$V_{OUTPP} \geq$ 200 mV	8			GHz
f_{SCLKIN}	Serial Clock Input Frequency				20	MHz
VOD_{0dB}	Output Voltage Amplitude (see Table 1) (@ $V_{INPPmin}$) (See Figure 3, Note 9)	$f_{in} \leq$ 6.0 GHz $f_{in} \leq$ 8.0 GHz	300 200	400 300		mV
t_{PE}	Pre−Emphasis Width, tested at −12dB Pre−Emphasis			130		ps
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 8)		1050		V_{CC}	mV
t_{PLH}, t_{PHL}	Propagation Delay to Differential Outputs, 1 GHz, measured at differential cross−point	IN/$\overline{IN}$ to Q/$\overline{Q}$ SCLKIN to SCLKOUT	150	200 5	250 10	ps ns
t_{DC}	Output Clock Duty Cycle (Reference Duty Cycle = 50%)	$f_{in} \leq$ 5.0 GHz	45	50	55	%
t_{s1} t_{s2} t_{s3}	Setup Time @ 50 MHz (Figures 9 and 10)	SDIN to SCLKIN SCLKIN to SLOAD SLOAD to IN/$\overline{IN}$	5 5 10			ns
t_{h1} t_{h2} t_{h3}	Hold Time @ 50 MHz (Figures 9 and 10)	SDIN to SCLKIN SCLKIN to SLOAD	1 2			ns
t_{PW_SLOAD}	SLOAD Minimum Pulse Width (Figure 10)		6			ns
t_{JITTER}	RJ − Output Random Jitter (Note 11) $f_{in} \leq$ 8.0 GHz DJ − Residual Output Deterministic Jitter (Note 12) (EQ = 0, PE = 0 dB) FR4 ≤ 3”, f ≤ 12.5 Gbps (Figures 15 and 16) FR4 = 12”, f ≤ 6.5 Gbps			0.1	0.8 10 10	ps rms ps pk−pk
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 9)		100		1200	mV
t_r, t_f	Output Rise/Fall Times @ 1 GHz (20% − 80%), Q, $\overline{Q}$			35	50	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured using a 400 mV source, 50% duty cycle clock source. All output loading with external 50 Ω to V_{CC}. Input edge rates 40 ps. (20% − 80%); PE = 0 dB, EQEN = 0
9. Input / Output voltage swing is a single−ended measurement operating in differential mode.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.
11. Additive RMS jitter with 50% duty cycle Clock signal.
12. Peak−to−Peak jitter with input NRZ data at PRBS23.

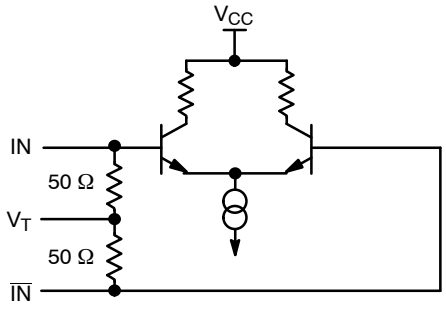


Figure 5. Input Structure

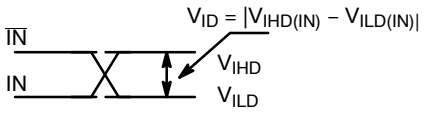


Figure 6. Differential Inputs Driven Differentially

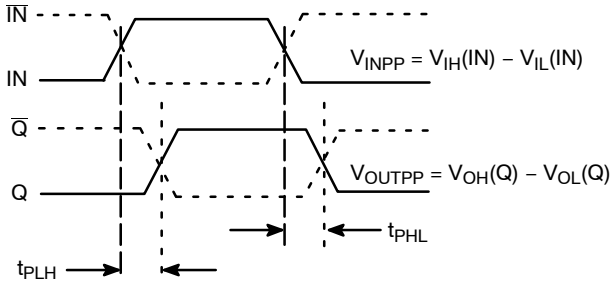


Figure 7. AC Reference Measurement

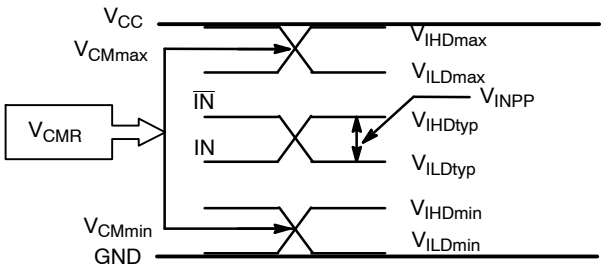


Figure 8. V_{CMR} Diagram

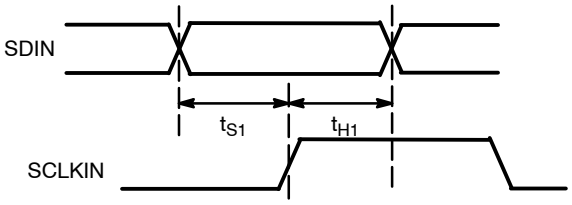


Figure 9. SDIN/SCLKIN Setup and Hold Time

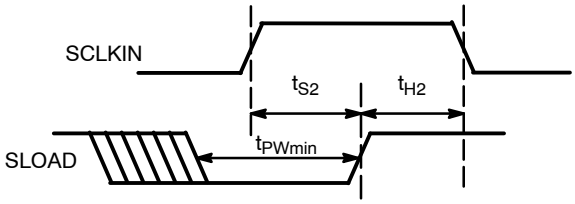


Figure 10. SLOAD Set−Up and Hold and t_{PWmin}

APPLICATION INFORMATION

Data Inputs

The differential IN/$\overline{IN}$ inputs of the NB7VPQ16M can accept LVPECL, CML, and LVDS signal levels. The limitations for a differential input signal (LVDS, LVPECL, or CML) is a minimum input swing of 100 mV (single−ended measurement). Within this condition, the input HIGH voltage, V_{IH}, can range from V_{CC} down to 1.1 V. Example interfaces are illustrated in Figure 17.

Serial Data Interface

The Serial Data Interface (SDI) logic is implemented with a 5−bit shift register scheme. The register shifts once per rising edge of the SCLKIN input. The serial data input SDIN must meet setup and hold timing as specified in the AC table. The configuration latches will capture the value of the shift register on the Low−to−High edge of the SLOAD input. The most significant bit (MSB) is loaded first. See the programming timing diagram for more information.

SDIN / SCLKIN

SDIN is the Serial Data input pin; SCLKIN is the Serial Clock input pin.

SLOAD

The SLOAD pin performs the DAC latch function. When LOW or left open, the DAC latch will pass the shift register outputs to the input of the DAC and the EQualizer ENable bit (EQEN). On the Low−to−HIGH transition of SLOAD, the input to the 4−bit DAC is locked to the state prior to when SLOAD went HIGH, and will set the EQualizer ENable bit. The DAC does not get programmed until SLOAD goes HIGH. The SLOAD pin must remain in a HIGH state to maintain the DAC Pre−Emphasis and the EQEN settings. A LOW or open state resets the DAC to 0 db Pre−Emphasis setting and disables the EQEN bit, regardless of SDIN and SCLKIN values. The SLOAD function is asynchronous.

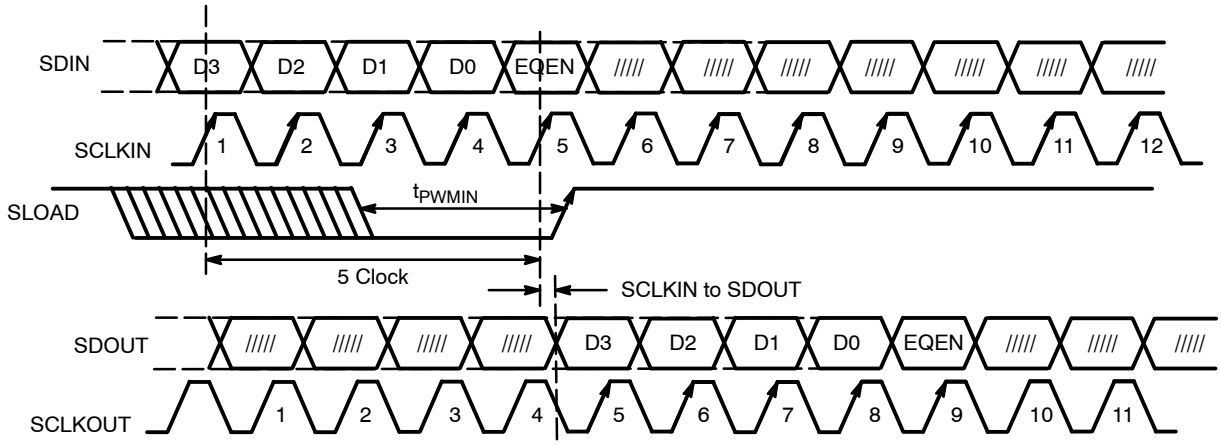


Figure 11. Timing Diagram for Single Channel

Pre−Emphasis Selection

The Pre−Emphasis buffer is controlled using a serial bus via the SDIN (Serial Data In) and SCLKIN (Serial Clock In) control inputs and contains circuitry which provides sixteen programmable pre−emphasis levels to control the output compensation. The 4−bits (D3:D0) digitally select 0 dB through 12 dB of Pre−Emphasis compensation (see Table 1). The default state at start−up is PE = 0 dB.

EQualization ENable (EQEN)

The EQualizer ENable (EQEN) allows for enabling the Equalizer function. The control of the Equalizer function is realized by setting the 5th bit, EQEN, of the 5−bit serial data. When EQEN is set Low (or open), the IN/$\overline{IN}$ inputs bypass the Equalizer. When EQEN is set High, the IN/$\overline{IN}$ inputs flow through the Equalizer. The default state at start−up is EQEN = LOW.

Q/$\overline{Q}$ Outputs

The differential outputs of the NB7VPQ16M, Q and $\overline{Q}$, utilize Common Mode Logic (CML) architecture. The outputs are designed to drive differential transmission lines with nominal 50 Ω characteristic impedance. External termination with a 50 Ω resistor to V_{CC} is recommended. See Figures 22 and 23 for output termination scheme. Alternatively, 100 Ω line−to−line termination is also acceptable.

Power Supply Bypass information

A clean power supply will optimize the performance of the NB7VPQ16M. The device provides separate V_{CCD} and V_{CC} power supply pins for the digital circuitry and CML outputs. Placing a 0.01 μF to 0.1 μF bypass capacitor on each V_{CC} and V_{CCD} Pin to ground will help ensure a noise free power supply. The purpose of this design technique is to isolate the CMOS digital switching noise from the high speed input/output path.

CASCADE APPLICATION

SDOUT/SCLKOUT

SDOUT is the Serial Data output pin; SCLKOUT is the Serial Clock output pin. These pins are the outputs of the 5−bit SDI shift register and will produce the SDIN/SCLKIN signals after five serial clock cycles, see Figure 12. The purpose of SDOUT and SCLKOUT is for use in cascade applications, described below.

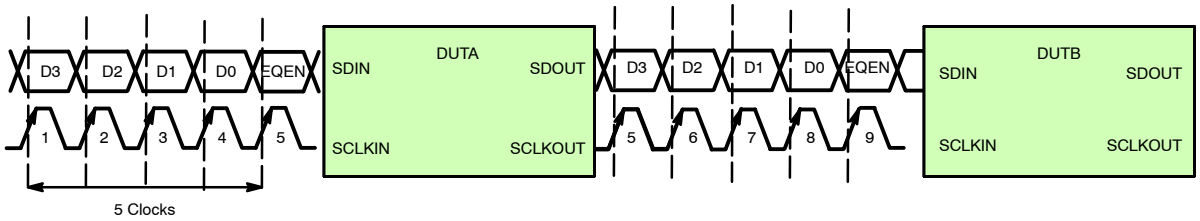


Figure 12. Simplified Cascaded Serial Data/Clock Timing Diagram

Cascaded Applications

The NB7VPQ16M can be cascaded with multiple NB7VPQ16Ms in series for various Equalizer/Pre−Emphasis applications, as shown in Figure 13.

Serial Data In, SDINA, is clocked with SCLKINA into the cascaded chain of the Pre−Emphasis and equalizer shift registers, (DUTA, DUTB and DUTC), 5−bits per register. Upon the rising edge of the 5th clock of SCLKINA, the first valid data bit (D3) and 5th clock will exit DUTA from SDOUTA and SCLKOUTA and will be present at SDINB and SCLKINB of DUTB and so on.

When SLOAD is brought LOW, the PE shift registers of all devices are enabled and data is written into the NB7VPQ16Ms with the contents of the PE shift registers. When the data transfer is complete, SLOAD is brought HIGH and all NB7VPQ16Ms are updated simultaneously. After the PE control bits are clocked into their appropriate registers, the Low−to−High transition of SLOAD will latch the data bits for the Pre−Emphasis DACs.

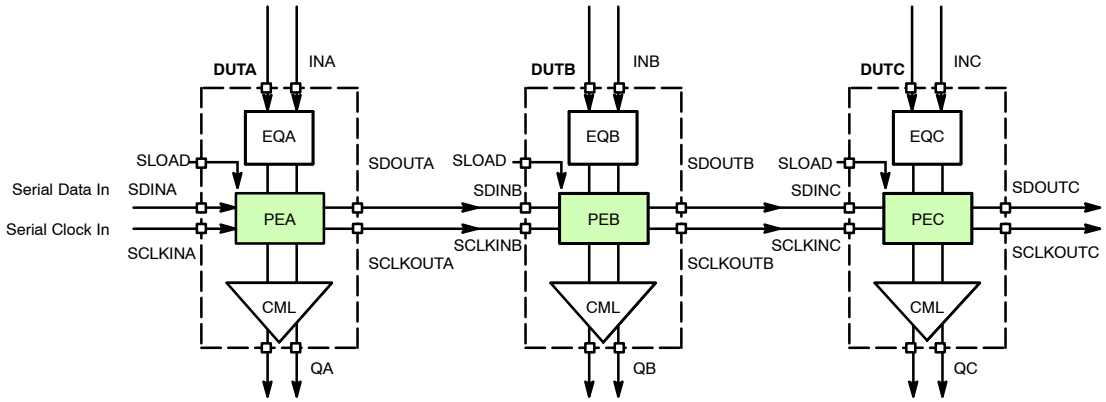


Figure 13. Simplified Cascaded Logic Diagram

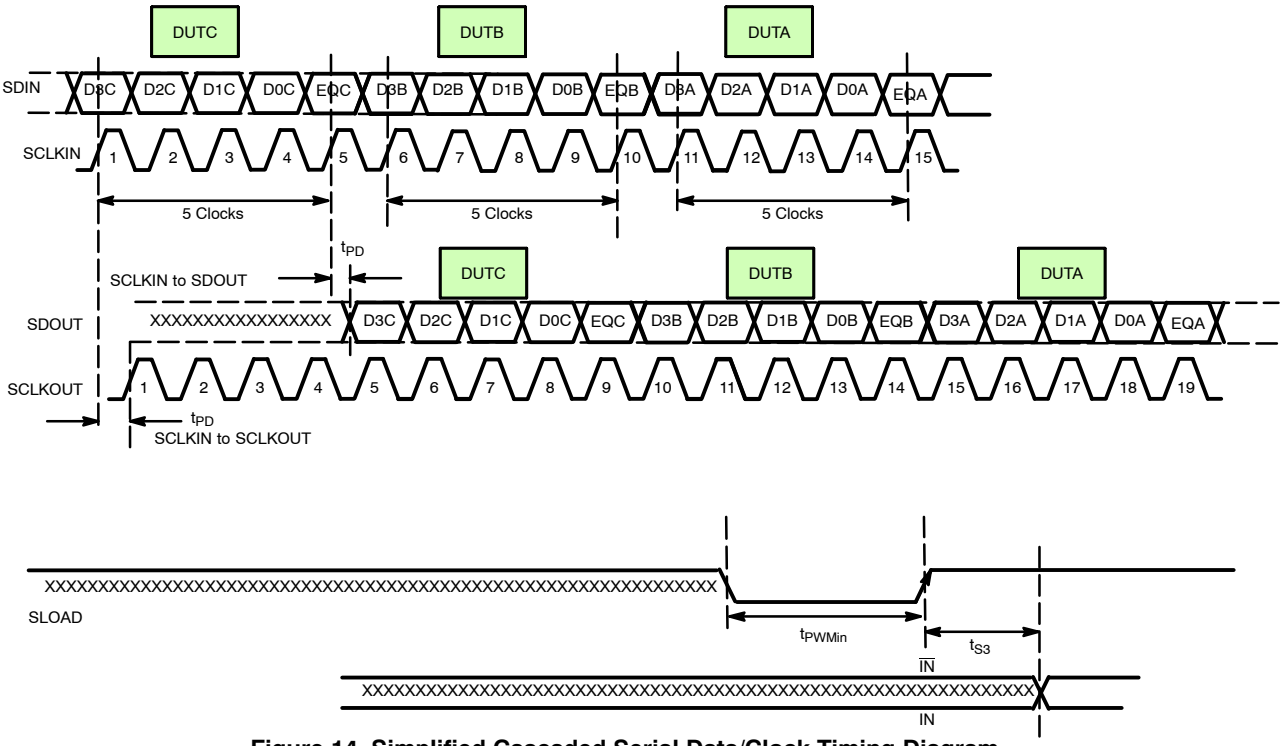


Figure 14. Simplified Cascaded Serial Data/Clock Timing Diagram

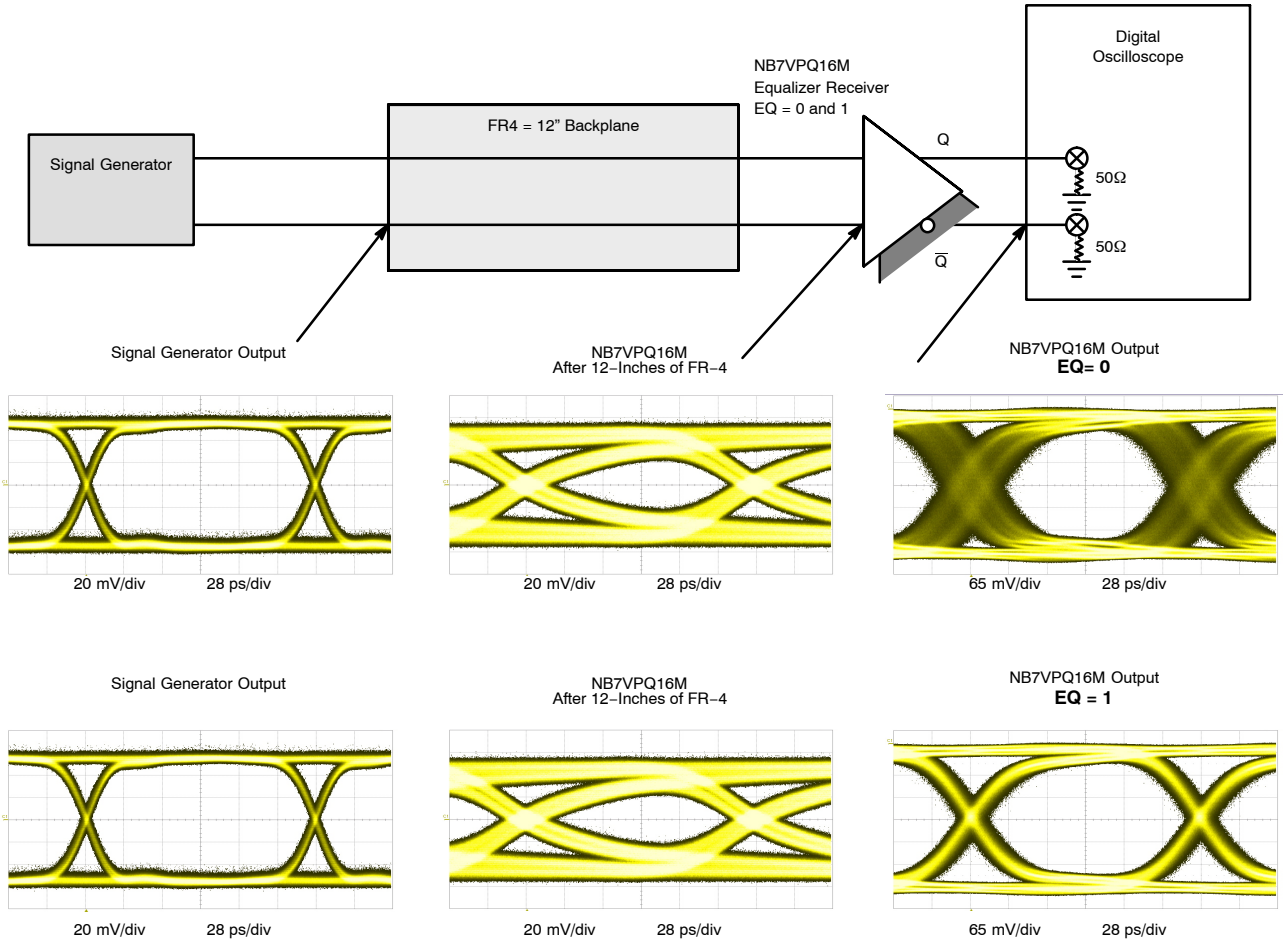


Figure 15. Typical NB7VPQ16M Equalizer Application and Interconnect; Eye Diagrams with PRBS23 Pattern at 6 Gbps

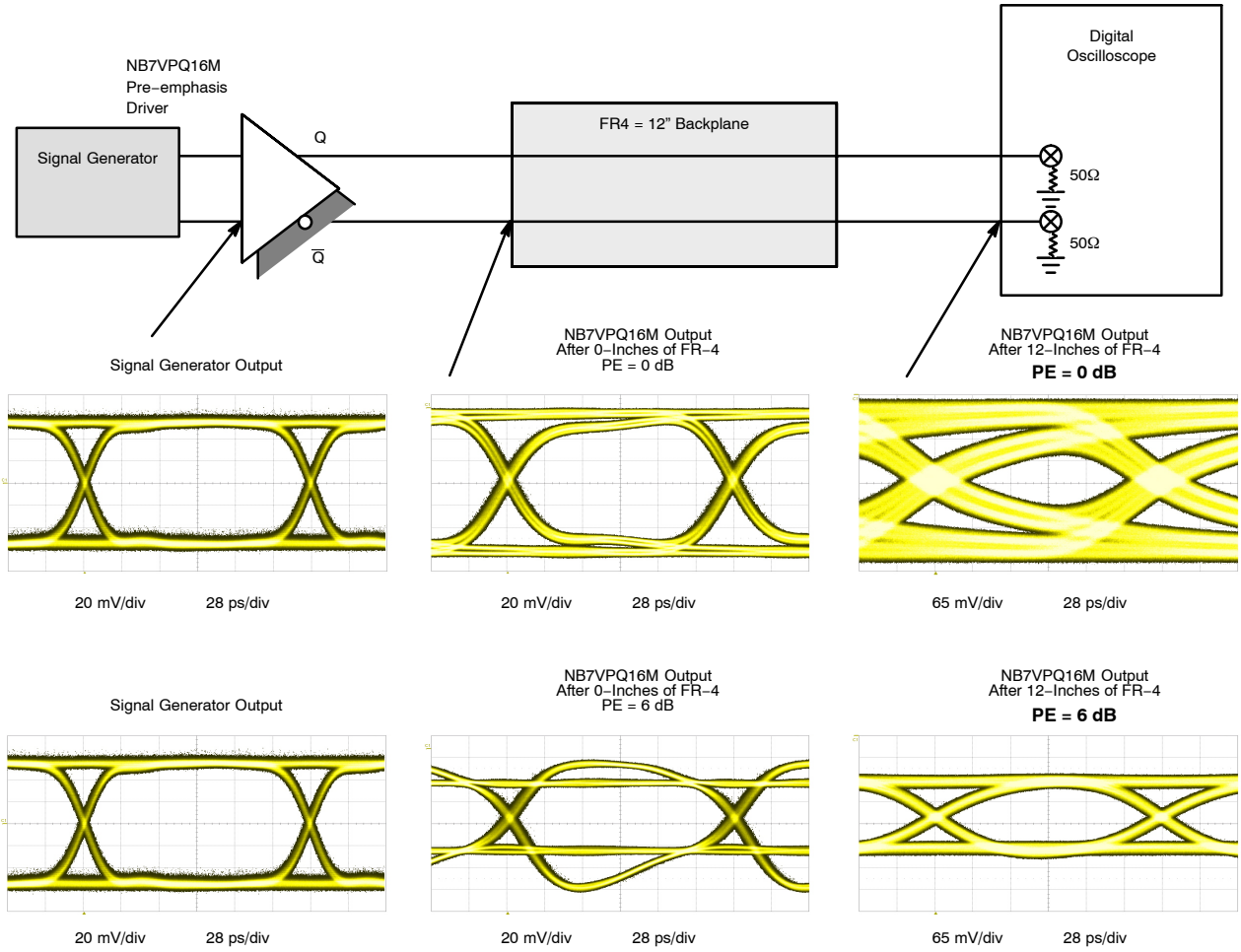


Figure 16. Typical NB7VPQ16M Pre−Emphasis Application Interconnect; Eye Diagrams with PRBS23 Pattern at 6 Gbps Without and With Pre−Emphasis

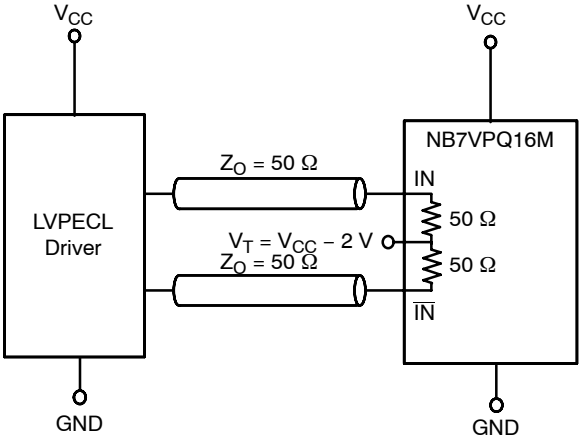


Figure 17. LVPECL Interface

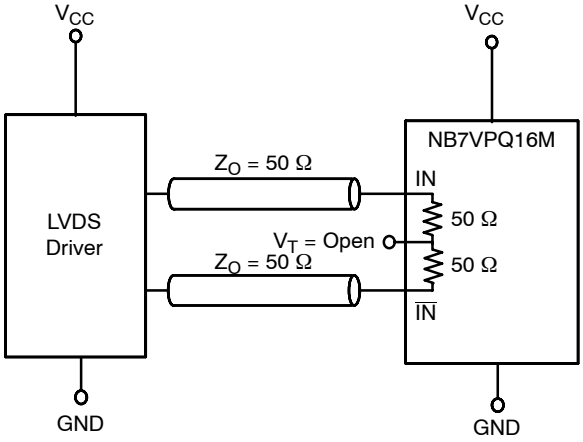


Figure 18. LVDS Interface

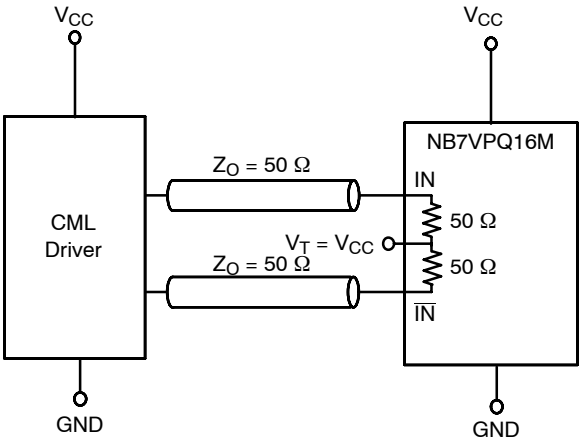


Figure 19. Standard 50 Ω Load CML Interface

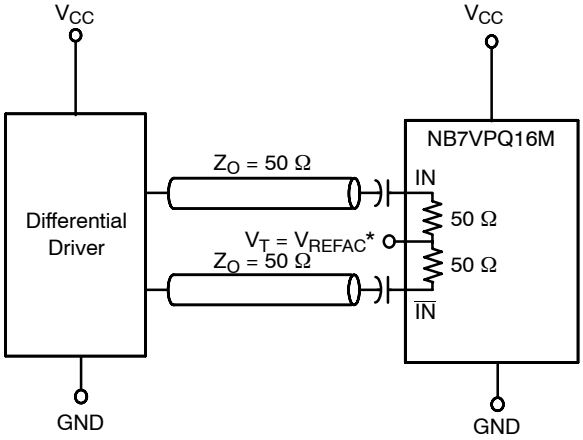


Figure 20. Capacitor−Coupled Differential Interface (VT Connected to External V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

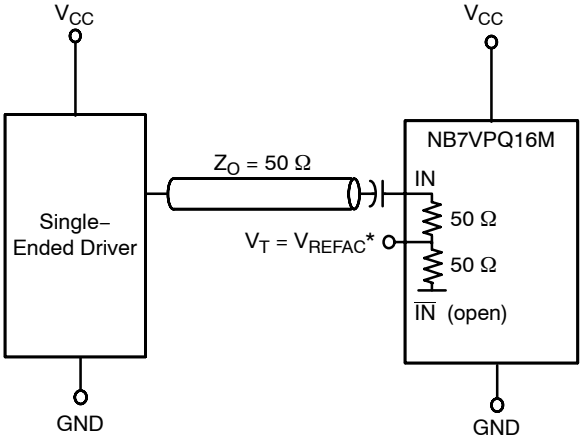


Figure 21. Capacitor−Coupled Single−Ended Interface (VT Connected to External V_{REFAC})

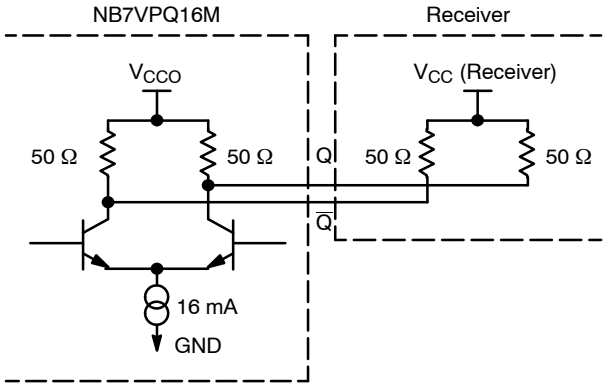


Figure 22. Typical CML Output Structure and Termination

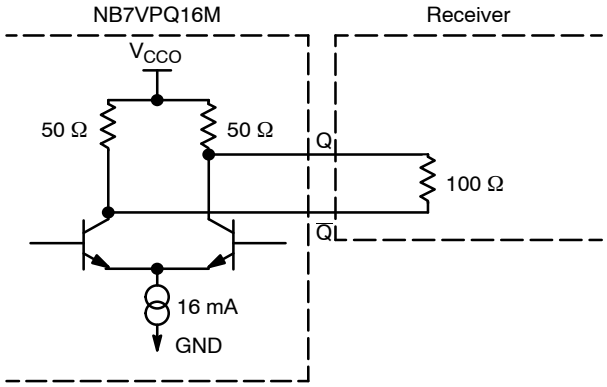


Figure 23. Alternative Output Termination

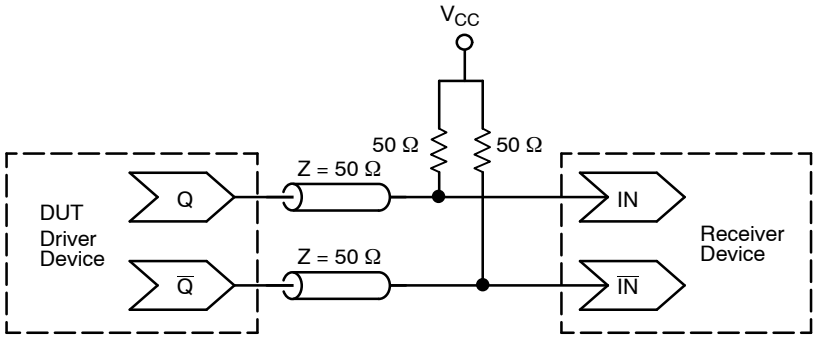


Figure 24. Typical Termination for CML Output Driver and Device Evaluation

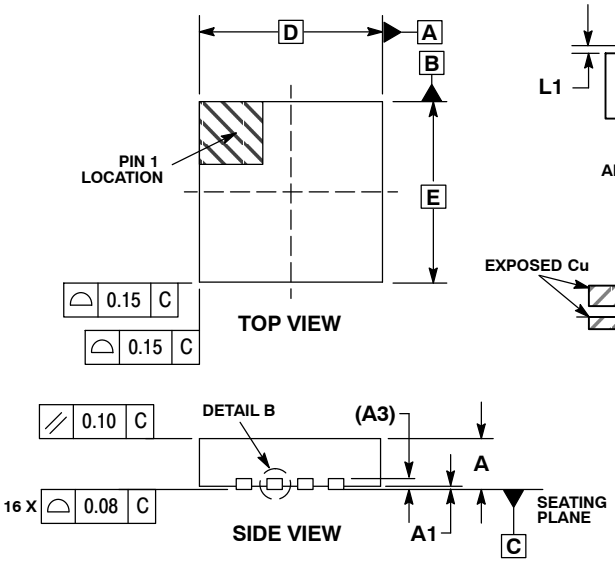
ORDERING INFORMATION

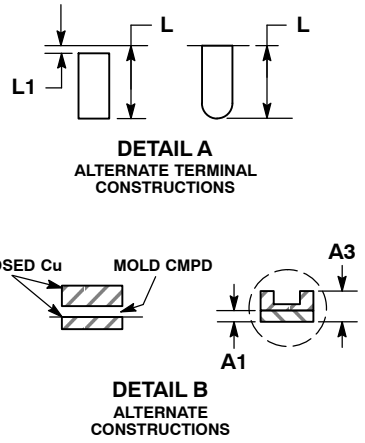
Device	Package	Shipping†
NB7VPQ16MMNG	QFN−16 (Pb−free)	123 Units / Rail
NB7VPQ16MMNTXG	QFN−16 (Pb−free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

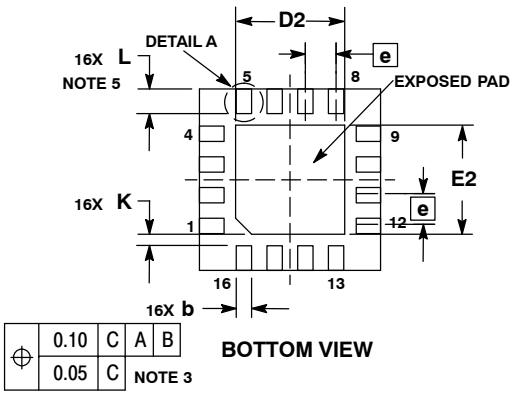
16 PIN QFN
CASE 485G−01
ISSUE D



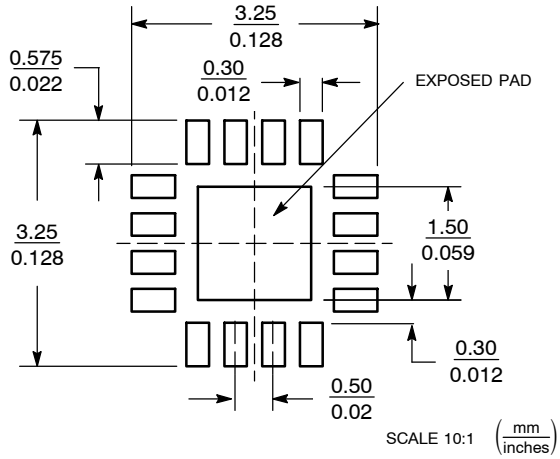


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50
L1	0.00	0.15



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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