

# NTMS10P02R2

## Power MOSFET -10 Amps, -20 Volts P-Channel Enhancement-Mode Single SOIC-8 Package

### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature SOIC-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SOIC-8 Mounting Information Provided
- Pb-Free Package is Available

### Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-20	Vdc
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 12$	Vdc
Thermal Resistance – Junction-to-Ambient (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $25^\circ\text{C}$ Continuous Drain Current @ $70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 3)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	50 2.5 -10 -8.0 0.6 -5.5 -50	$^\circ\text{C/W}$ W A A W A A
Thermal Resistance – Junction-to-Ambient (Note 2) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Continuous Drain Current @ $25^\circ\text{C}$ Continuous Drain Current @ $70^\circ\text{C}$ Maximum Operating Power Dissipation Maximum Operating Drain Current Pulsed Drain Current (Note 3)	$R_{\theta JA}$ $P_D$ $I_D$ $I_D$ $P_D$ $I_D$ $I_{DM}$	80 1.6 -8.8 -6.4 0.4 -4.5 -44	$^\circ\text{C/W}$ W A A W A A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = -20$ Vdc, $V_{GS} = -4.5$ Vdc, Peak $I_L = 5.0$ Apk, $L = 40$ mH, $R_G = 25$ $\Omega$ )	$E_{AS}$	500	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

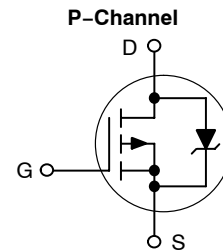
1. Mounted onto a 2" square FR-4 Board  
(1 in sq, Cu 0.06" thick single sided),  $t = 10$  seconds.
2. Mounted onto a 2" square FR-4 Board  
(1 in sq, Cu 0.06" thick single sided),  $t =$  steady state.
3. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2%.



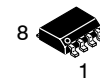
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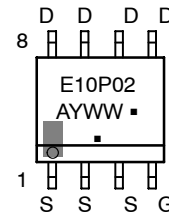
**-10 AMPERES  
-20 VOLTS  
14 m $\Omega$  @  $V_{GS} = -4.5$  V**



### MARKING DIAGRAM & PIN ASSIGNMENT



SOIC-8  
CASE 751  
STYLE 12



E10P02 = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS10P02R2	SOIC-8	2500/Tape & Reel
NTMS10P02R2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMS10P02R2

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted) (Note 4)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	-20 -	- -12.1	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = -20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 25°C) (V <sub>DS</sub> = -20 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 70°C)	I <sub>DSS</sub>	- -	- -	-1.0 -5.0	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = -12 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	-100	nAdc
Gate-Body Leakage Current (V <sub>GS</sub> = +12 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	100	nAdc

### ON CHARACTERISTICS

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc) Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	-0.6 -	-0.88 2.8	-1.20 -	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -10 Adc) (V <sub>GS</sub> = -2.5 Vdc, I <sub>D</sub> = -8.8 Adc)	R <sub>DS(on)</sub>	- -	0.012 0.017	0.014 0.020	Ω
Forward Transconductance (V <sub>DS</sub> = -10 Vdc, I <sub>D</sub> = -10 Adc)	g <sub>FS</sub>	-	30	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = -16 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	3100	3640	pF
Output Capacitance		C <sub>OSS</sub>	-	1100	1670	
Reverse Transfer Capacitance		C <sub>rss</sub>	-	475	1010	

### SWITCHING CHARACTERISTICS (Notes 5 & 6)

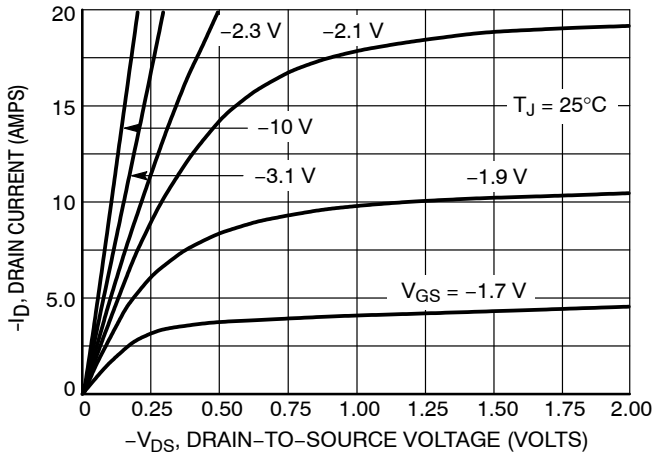
Turn-On Delay Time	(V <sub>DD</sub> = -10 Vdc, I <sub>D</sub> = -1.0 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	25	35	ns
Rise Time		t <sub>r</sub>	-	40	65	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	110	190	
Fall Time		t <sub>f</sub>	-	110	190	
Turn-On Delay Time	(V <sub>DD</sub> = -10 Vdc, I <sub>D</sub> = -10 Adc, V <sub>GS</sub> = -4.5 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	-	25	-	ns
Rise Time		t <sub>r</sub>	-	100	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	100	-	
Fall Time		t <sub>f</sub>	-	125	-	
Total Gate Charge	(V <sub>DS</sub> = -10 Vdc, V <sub>GS</sub> = -4.5 Vdc, I <sub>D</sub> = -10 Adc)	Q <sub>tot</sub>	-	48	70	nC
Gate-Source Charge		Q <sub>gs</sub>	-	6.5	-	
Gate-Drain Charge		Q <sub>gd</sub>	-	17	-	

### BODY-DRAIN DIODE RATINGS (Note 5)

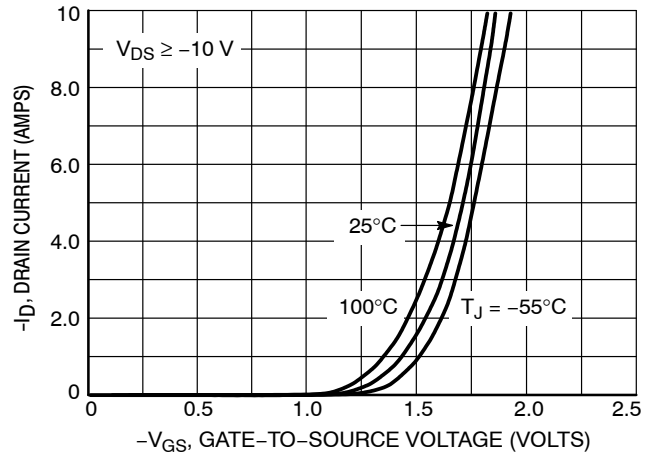
Diode Forward On-Voltage	(I <sub>S</sub> = -2.1 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = -2.1 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	-0.72 -0.60	-1.2 -	Vdc
Diode Forward On-Voltage	(I <sub>S</sub> = -10 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = -10 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	- -	-0.90 -0.75	- -	Vdc
Reverse Recovery Time	(I <sub>S</sub> = -2.1 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	-	65	100	ns
		t <sub>a</sub>	-	25	-	
		t <sub>b</sub>	-	40	-	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	-	0.075	-	μC

4. Handling precautions to protect against electrostatic discharge is mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

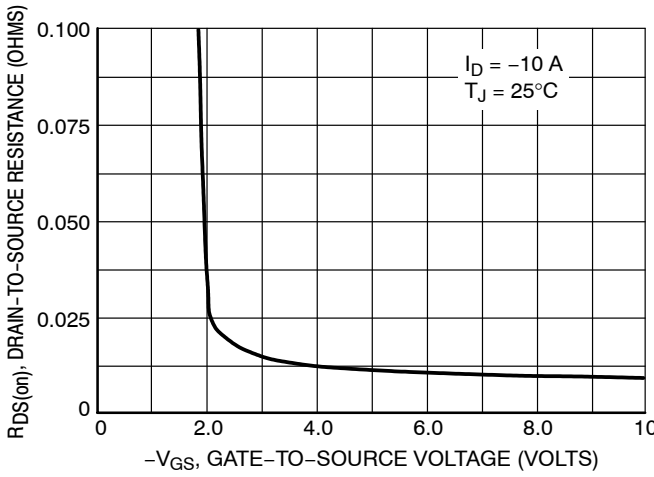
# NTMS10P02R2



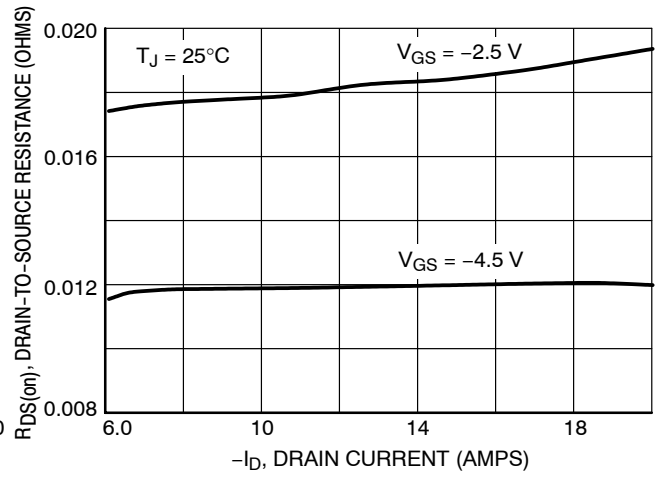
**Figure 1. On-Region Characteristics**



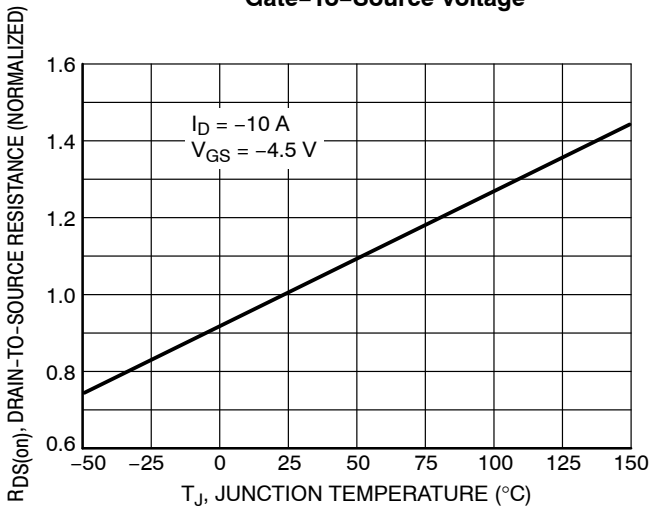
**Figure 2. Transfer Characteristics**



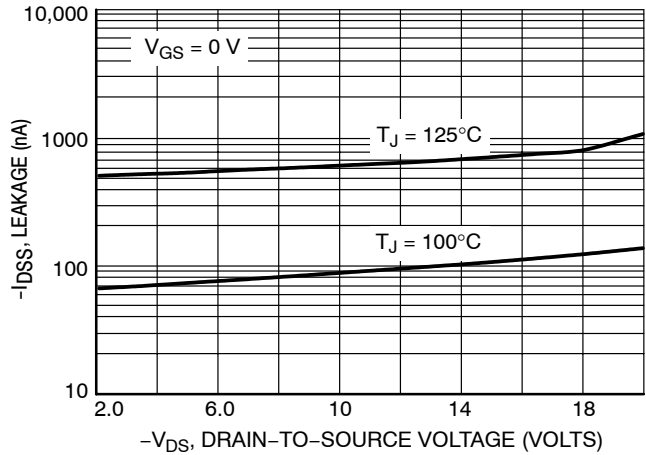
**Figure 3. On-Resistance versus Gate-To-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-To-Source Leakage Current versus Voltage**

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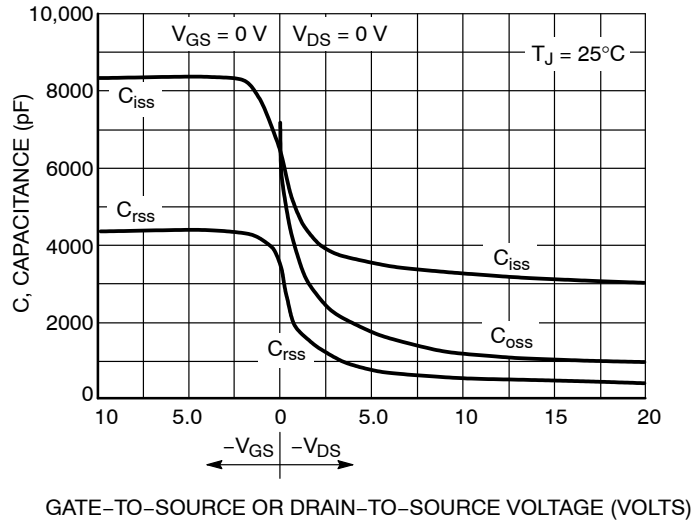


Figure 7. Capacitance Variation

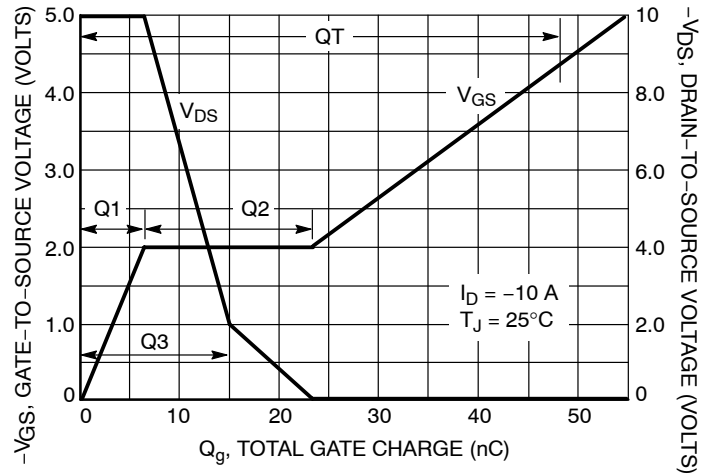


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

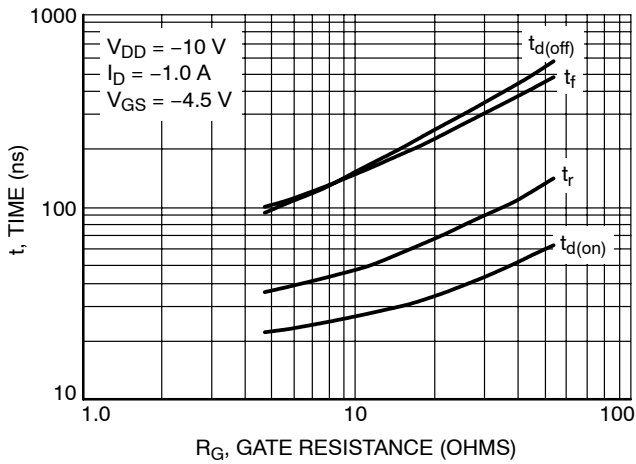


Figure 9. Resistive Switching Time Variation versus Gate Resistance

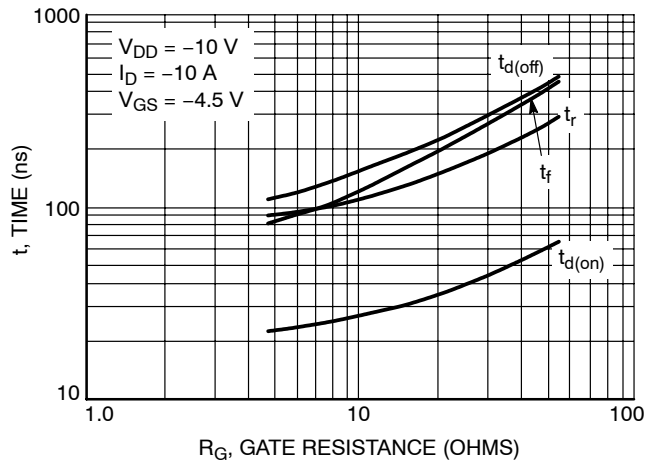


Figure 10. Resistive Switching Time Variation versus Gate Resistance

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## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

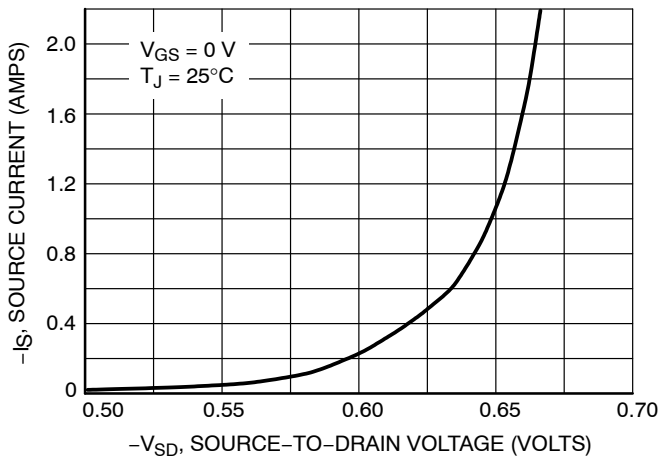


Figure 11. Diode Forward Voltage versus Current

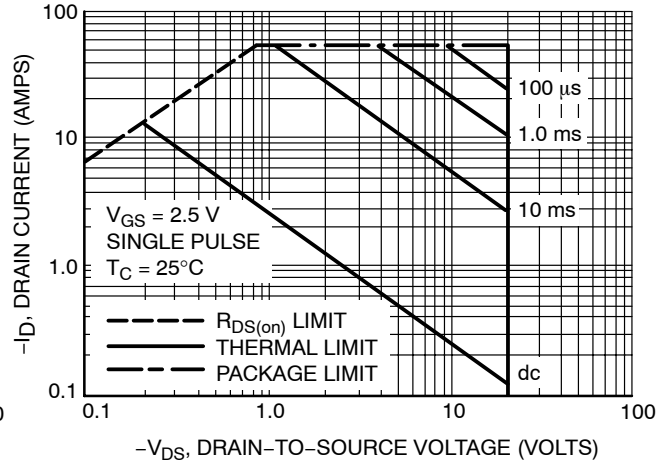


Figure 12. Maximum Rated Forward Biased Safe Operating Area

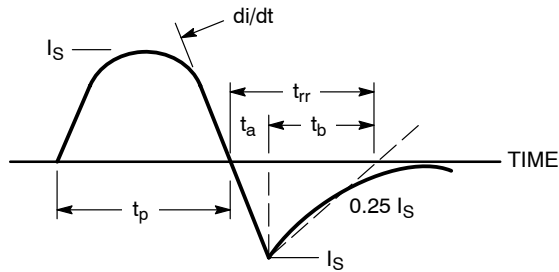


Figure 13. Diode Reverse Recovery Waveform

## TYPICAL ELECTRICAL CHARACTERISTICS

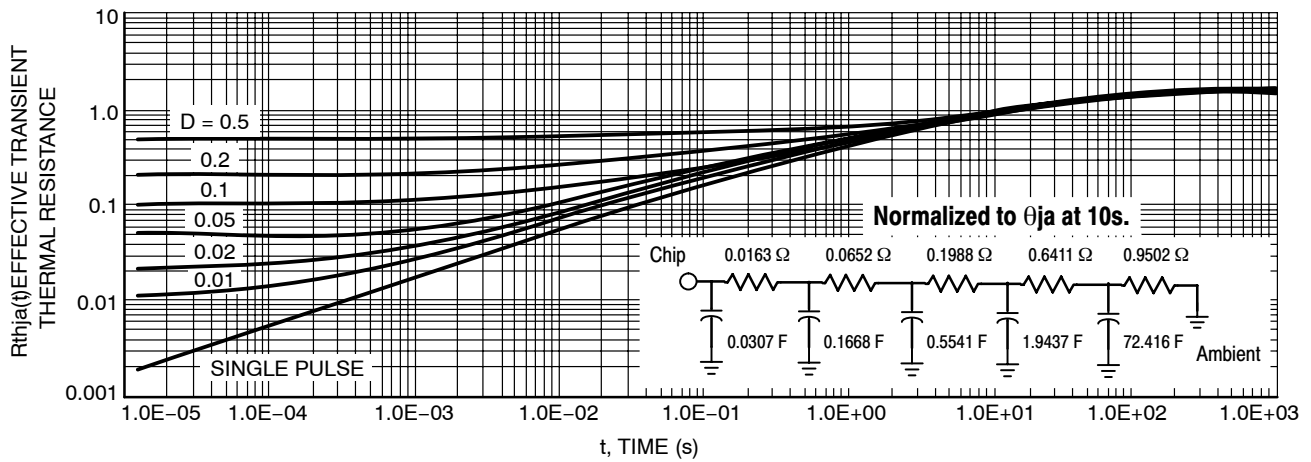
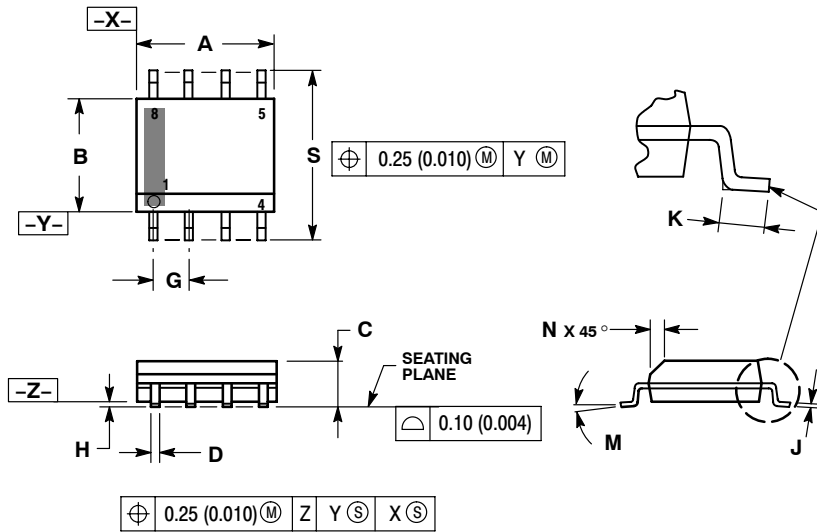


Figure 14. Thermal Response

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## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AG



**NOTES:**

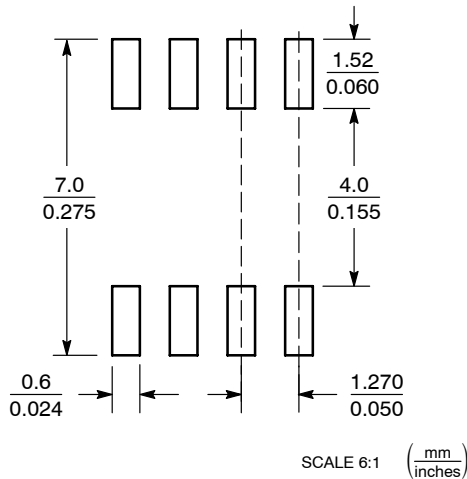
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

**STYLE 12:**

1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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