

# 2.5 V or 3.3 V, 200 MHz, 1:18 Clock Distribution Buffer

## Features

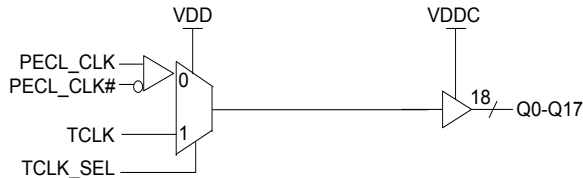
- 200 MHz clock support
- LVPECL or LVCMOS/LVTTL clock input
- LVCMOS/LVTTL compatible inputs
- 18 clock outputs: drive up to 36 clock lines
- 60 ps typical output-to-output skew
- Dual or single supply operation:
  - 3.3 V core and 3.3 V outputs
  - 3.3 V core and 2.5 V outputs
  - 2.5 V core and 2.5 V outputs
- Pin compatible with MPC940L, MPC9109
- Available in Commercial and Industrial temperature
- 32-pin TQFP package

## Functional Description

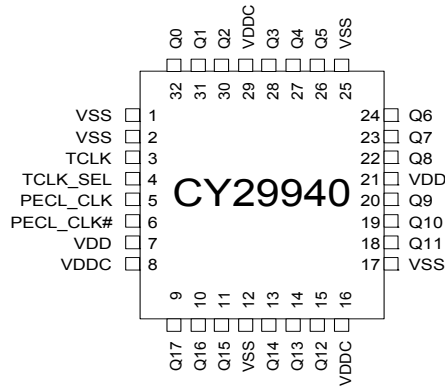
The CY29940 is a low-voltage 200 MHz clock distribution buffer with the capability to select either a differential LVPECL or a LVCMOS/LVTTL compatible input clock. The two clock sources can be used to provide for a test clock as well as the primary system clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5 V or 3.3 V LVCMOS/LVTTL compatible and can drive 50 Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:36. Low output-to-output skews make the CY29940 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

For a complete list of related documentation, [click here](#).

## Block Diagram



## Pin Configuration



## Pin Description

Pin	Name	PWR	I/O [1]	Description
5	PECL_CLK		I, PU	PECL input clock
6	PECL_CLK#		I, PD	PECL input clock
3	TCLK		I, PD	External reference/test clock input
9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32	Q(17:0)	VDDC	O	Clock outputs
4	TCLK_SEL		I, PD	Clock Select Input. When LOW, PECL clock is selected and when HIGH TCLK is selected.
8, 16, 29	VDDC			3.3 V or 2.5 V power supply for output clock buffers
7, 21	VDD			3.3 V or 2.5 V power supply
1, 2, 12, 17, 25	VSS			Common ground

**Note**

1. PD = Internal Pull-Down, PU = Internal Pull-up

### Maximum Ratings

Exceeding the maximum ratings<sup>[2]</sup> may impair the useful life of the device. User guidelines are not tested.

- Maximum input voltage relative to V<sub>SS</sub> ..... V<sub>SS</sub> – 0.3 V
- Maximum input voltage relative to V<sub>DD</sub> ..... V<sub>DD</sub> + 0.3 V
- Storage temperature ..... –65 °C to +150 °C
- Operating temperature ..... –40 °C to +85 °C
- Maximum ESD protection ..... 2 kV

- Maximum power supply ..... 5.5 V
- Maximum input current ..... ±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V<sub>SS</sub> or V<sub>DD</sub>).

### DC Parameters

V<sub>DD</sub> = 3.3 V ± 5% or 2.5 V ± 5%, V<sub>DDC</sub> = 3.3 V ± 5% or 2.5 V ± 5%, T<sub>A</sub> = –40 °C to +85 °C

Parameter <sup>[2]</sup>	Description	Conditions	Min	Typ	Max	Unit
V <sub>IL</sub>	Input low voltage		V <sub>SS</sub>	–	0.8	V
V <sub>IH</sub>	Input high voltage		2.0	–	V <sub>DD</sub>	V
I <sub>IL</sub>	Input low current <sup>[3]</sup>		–	–	–200	µA
I <sub>IH</sub>	Input high current <sup>[3]</sup>		–	–	200	µA
V <sub>PP</sub>	Peak-to-peak input voltage PECL_CLK		500	–	1000	mV
V <sub>CMR</sub>	Common mode range <sup>[4]</sup> PECL_CLK	V <sub>DD</sub> = 3.3 V	V <sub>DD</sub> – 1.4	–	V <sub>DD</sub> – 0.6	V
		V <sub>DD</sub> = 2.5 V	V <sub>DD</sub> – 1.0	–	V <sub>DD</sub> – 0.6	V
V <sub>OL</sub>	Output low voltage <sup>[5, 6, 7]</sup>	I <sub>OL</sub> = 20 mA	–	–	0.5	V
V <sub>OH</sub>	Output high voltage <sup>[5, 6, 7]</sup>	I <sub>OH</sub> = –20 mA, V <sub>DDC</sub> = 3.3 V	2.4	–	–	V
		I <sub>OH</sub> = –20 mA, V <sub>DDC</sub> = 2.5 V	1.8	–	–	V
I <sub>DDQ</sub>	Quiescent supply current		–	5	7	mA
I <sub>DD</sub>	Dynamic supply current	V <sub>DD</sub> = 3.3 V, Outputs at 150 MHz, C <sub>L</sub> = 15 pF	–	285	–	mA
		V <sub>DD</sub> = 3.3 V, Outputs at 200 MHz, C <sub>L</sub> = 15 pF	–	335	–	
		V <sub>DD</sub> = 2.5 V, Outputs at 150 MHz, C <sub>L</sub> = 15 pF	–	200	–	
		V <sub>DD</sub> = 2.5 V, Outputs at 200 MHz, C <sub>L</sub> = 15 pF	–	240	–	
Z <sub>out</sub>	Output impedance	V <sub>DD</sub> = 3.3 V	8	12	16	Ω
		V <sub>DD</sub> = 2.5 V	10	15	20	
C <sub>in</sub>	Input capacitance		–	4	–	pF

### Thermal Resistance

Parameter <sup>[8]</sup>	Description	Test Conditions	32-pin TQFP	Unit
θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	67	°C/W
θ <sub>JC</sub>	Thermal resistance (junction to case)		28	°C/W

**Notes**

2. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. The VCMR is the difference from the most positive side of the differential input signal. Normal operation is obtained when the "High" input is within the VCMR range and the input lies within the VPP specification. Driving series or parallel terminated 50 Ω (or 50 Ω to V<sub>DD</sub>/2) transmission lines
5. Outputs driving 50 Ω transmission lines.
6. See Figure 1 on page 5 and Figure 2 on page 5.
7. 50% input duty cycle.
8. These parameters are guaranteed by design and are not tested.

**AC Parameters<sup>[9]</sup>**
 $V_{DD} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ,  $V_{DDC} = 3.3\text{ V} \pm 5\%$  or  $2.5\text{ V} \pm 5\%$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ 

Parameter	Description	Conditions	Min	Typ	Max	Unit	
$F_{max}$	Input frequency		–	–	200	MHz	
$t_{PD}$	PECL_CLK to Q Delay <sup>[10, 11, 12]</sup> $\leq 150\text{ MHz}$	$V_{DD} = 3.3\text{ V}, 85\text{ }^\circ\text{C}$	$t_{PHL}$	2.0	–	3.2	ns
			$t_{PLH}$	2.1	–	3.4	
		$V_{DD} = 3.3\text{ V}, 70\text{ }^\circ\text{C}$	$t_{PHL}$	1.9	–	3.1	
			$t_{PLH}$	2.0	–	3.2	
		$V_{DD} = 2.5\text{ V}, 85\text{ }^\circ\text{C}$	$t_{PHL}$	2.5	–	5.2	
			$t_{PLH}$	2.6	–	5	
		$V_{DD} = 2.5\text{ V}, 70\text{ }^\circ\text{C}$	$t_{PHL}$	2.5	–	5	
			$t_{PLH}$	2.6	–	5	
$t_{PD}$	LVCMOS to Q Delay <sup>[10, 11, 12]</sup> $\leq 150\text{ MHz}$	$V_{DD} = 3.3\text{ V}, 85\text{ }^\circ\text{C}$	$t_{PHL}$	1.9	–	3	ns
			$t_{PLH}$	2.0	–	3.2	
		$V_{DD} = 3.3\text{ V}, 70\text{ }^\circ\text{C}$	$t_{PHL}$	1.8	–	2.9	
			$t_{PLH}$	1.8	–	3.1	
		$V_{DD} = 2.5\text{ V}, 85\text{ }^\circ\text{C}$	$t_{PHL}$	2.5	–	4	
			$t_{PLH}$	2.5	–	4	
		$V_{DD} = 2.5\text{ V}, 70\text{ }^\circ\text{C}$	$t_{PHL}$	2.3	–	3.8	
			$t_{PLH}$	2.3	–	3.8	
$t_J$	Total jitter	$V_{DD} = 3.3\text{ V @ }150\text{ MHz}$	–	–	10	ps	
$F_{outDC}$	Output duty cycle <sup>[10, 11, 13]</sup>	$F_{CLK} < 134\text{ MHz}$	–	–	55	%	
		$F_{CLK} > 134\text{ MHz}$	–	–	60		
$T_{skew}$	Output-to-output skew <sup>[10, 11]</sup>	$V_{DD} = 3.3\text{ V}$	–	60	150	ps	
		$V_{DD} = 2.5\text{ V}$	–	–	200		
$T_{skew(PP)}$	Part-to-part skew <sup>[14]</sup>	PECL, $V_{DDC} = 3.3\text{ V}$	–	–	1.4	ns	
		PECL, $V_{DDC} = 2.5\text{ V}$	–	–	2.2		
$T_{skew(PP)}$	Part-to-part skew <sup>[14]</sup>	TCLK, $V_{DDC} = 3.3\text{ V}$	–	–	1.2	ns	
		TCLK, $V_{DDC} = 2.5\text{ V}$	–	–	1.7		
$T_{skew(PP)}$	Part-to-part skew <sup>[15]</sup>	PECL_CLK	–	–	850	ps	
		TCLK	–	–	750		
$t_R/t_F$	Output clocks rise/fall time <sup>[10, 11]</sup>	0.7 V to 2.0 V, $V_{DDC} = 3.3\text{ V}$	0.3	–	1.1	ns	
		0.5 V to 1.8 V, $V_{DDC} = 2.5\text{ V}$	0.3	–	1.2		

**Notes**

9. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
10. Outputs driving  $50\ \Omega$  transmission lines.
11. See [Figure 1 on page 5](#) and [Figure 2 on page 5](#).
12. Parameters tested @ 150 MHz.
13. 50% input duty cycle.
14. Across temperature and voltage ranges, includes output skew.
15. For a specific temperature and voltage, includes output skew.

Figure 1. LVCMOS\_CLK CY29940 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$

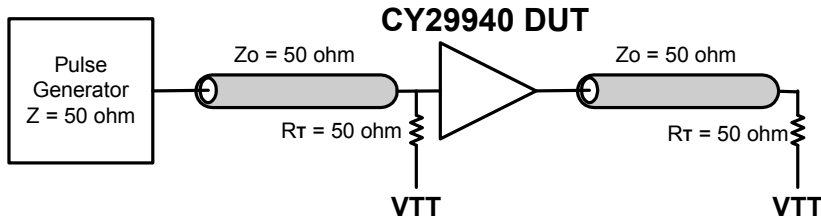


Figure 2. PECL\_CLK CY29940 Test Reference for  $V_{CC} = 3.3\text{ V}$  and  $V_{CC} = 2.5\text{ V}$

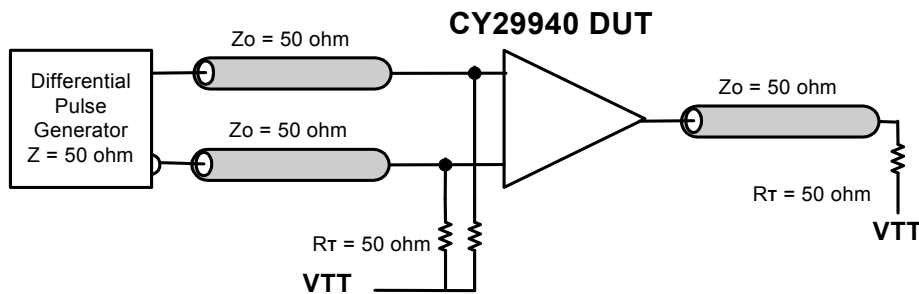


Figure 3. Propagation Delay (TPD) Test Reference

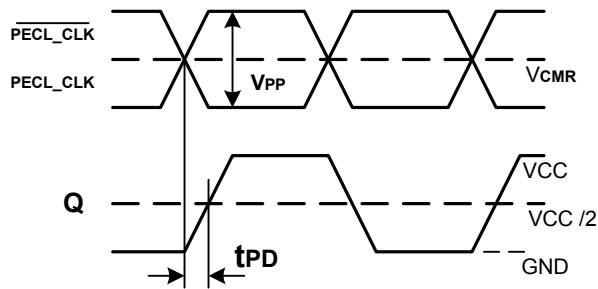
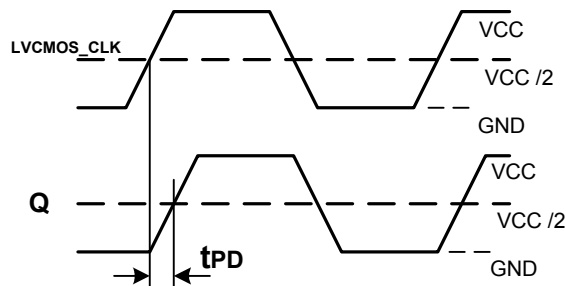
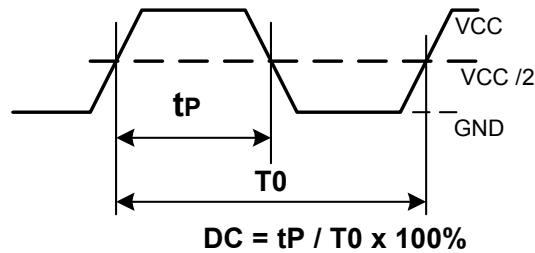


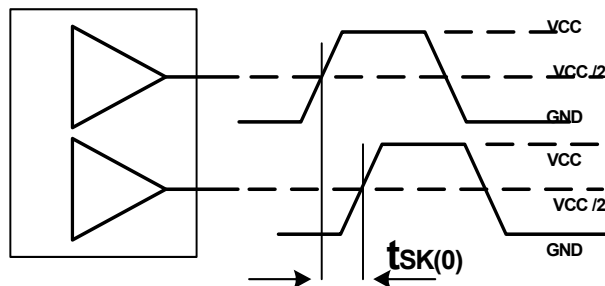
Figure 4. LVCMOS Propagation Delay (TPD) Test Reference



**Figure 5. Output Duty Cycle (FoutDC)**



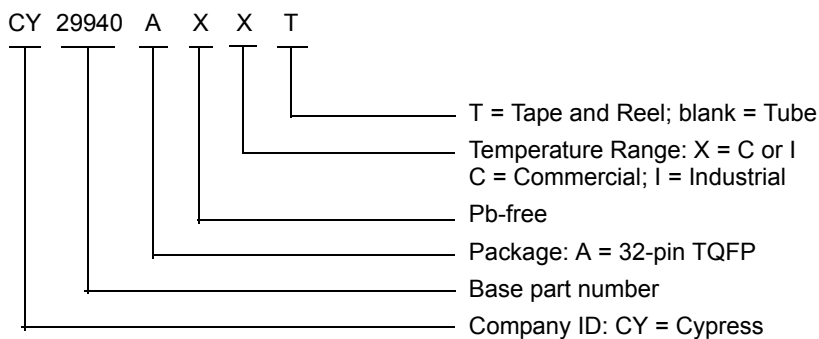
**Figure 6. Output-to-Output Skew tsk(0)**



## Ordering Information

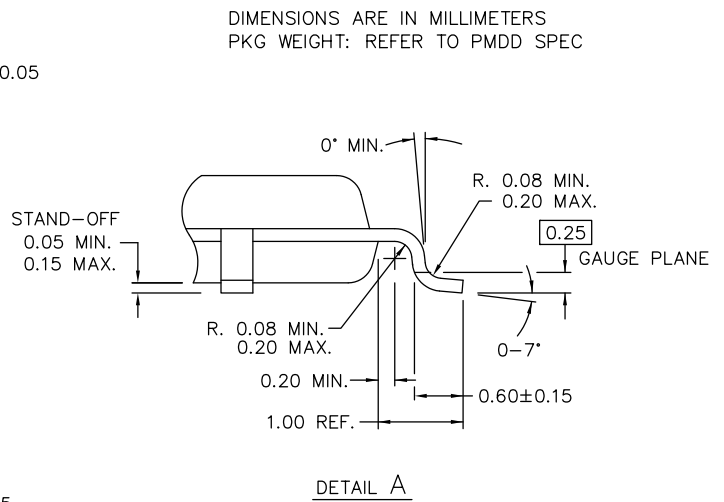
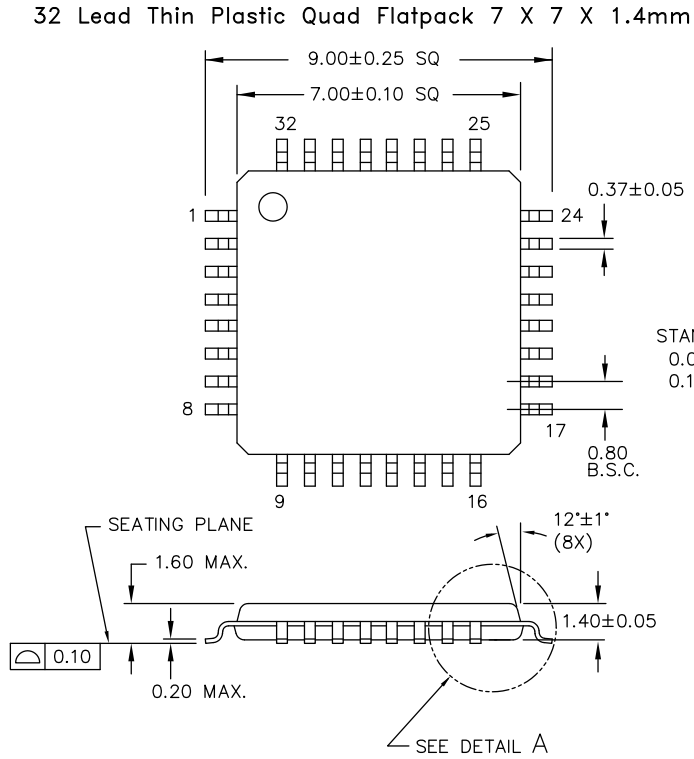
Part Number	Package Type	Production Flow
<b>Pb-free</b>		
CY29940AXI	32-pin TQFP	Industrial, -40 °C to +85 °C
CY29940AXIT	32-pin TQFP – Tape and Reel	Industrial, -40 °C to +85 °C
CY29940AXC	32-pin TQFP	Commercial, 0 °C to 70 °C
CY29940AXCT	32-pin TQFP – Tape and Reel	Commercial, 0 °C to 70 °C

## Ordering Code Definitions



Package Drawing and Dimensions

Figure 7. 32-pin TQFP 7 × 7 × 1.4 mm A32.14



51-85088 \*E

## Acronyms

Acronym	Description
ESD	electrostatic discharge
I/O	input/output
TQFP	thin quad flat package
LVC MOS	low voltage complementary metal oxide semiconductor
LVPECL	low-voltage positive emitter-coupled logic
LVTTL	low-voltage transistor-transistor logic
TQFP	thin quad flat pack

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kV	kilo Volts
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
mV	milli Volts
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
ps	pico seconds
V	Volts
W	Watts



## Document History Page

Document Title: CY29940, 2.5 V or 3.3 V, 200 MHz, 1:18 Clock Distribution Buffer Document Number: 38-07283				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	111094	02/01/02	BRK	New data sheet
*A	116776	08/15/02	HWT	Incorporate results of final characterization using corporate methods, added output impedance on page 3 and added output duty cycle on page 4. Updated <a href="#">Ordering Information</a> : Add commercial temperature range part numbers.
*B	122875	12/21/02	RBI	Add power up requirements to maximum rating information
*C	448379	See ECN	RGL	Add typical value for output-to-output skew Updated <a href="#">Ordering Information</a> : Added Lead-free devices.
*D	2899304	03/25/10	BASH / KVM	Updated <a href="#">Ordering Information</a> : Removed inactive parts. Updated <a href="#">Package Drawing and Dimensions</a> .
*E	3254185	05/11/2011	CXQ	Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template.
*F	3548252	03/12/2012	PURU	Changed LQFP to TQFP throughout document.
*G	4586288	12/03/2014	PURU	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, <a href="#">click here</a> ." at the end. Updated <a href="#">Package Drawing and Dimensions</a> : Updated <a href="#">Figure 7</a> (spec 51-85088 – Changed revision from *D to *E).
*H	4787038	06/04/2015	TAVA	Updated to new template. Completing Sunset Review.
*I	5258862	05/04/2016	PSR	Added <a href="#">Thermal Resistance</a> . Updated to new template. Completing Sunset Review.

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