256K-bit Serial Peripheral Interface FRAM
MB85RS256

A 256K-bit 1T1C-type FRAM equipped with a serial peripheral interface (SPI).
It is a nonvolatile memory that enables a large number of writing/reading cycles at high speed and with low power consumption.

* SPI: Serial Peripheral Interface

Overview

This product is a 32,768 words×8 bits FRAM (Ferroelectric Random Access Memory) that applies the ferroelectric process to form nonvolatile memory cells; it also utilizes the silicone gate CMOS process. It incorporates a high-speed serial peripheral interface. It enables space saving of one-quarter or less compared to our parallel product 256K (MB85R256) TSOP28-pin.

This product is capable of 10^{10} writing/reading cycles, which greatly exceeds the 10^5 or 10^6 cycles for Flash memory and EEPROM. In addition, writing is executed at high speed and does not require a writing completion waiting sequence. This enables utilization of FRAM advantages to applications to have it memorize by writing the final status for system power supply OFF in a short period and to reduce the process time when rewriting adjustments in system shipment.

Since this product has a short writing period, the power consumption for a single writing (power consumption×writing period) reaches approximately 1/7000 of the equivalent EEPROM product, realizing significant power saving.

Product Features

Major specifications

- Bit structure: 32,768 words×8 bits
- Power supply voltage for operation: 3.0V to 3.6V
- Power supply current for operation: 10mA @15MHz
- Operation frequency: 15MHz (Max.)
- Serial peripheral interface
- SPI mode 0 (0, 0) and mode 3 (1, 1) are supported.
- Package: SOL8, TSSOP14
- Temperature range for operation: −20℃ to +85℃

Fig.1 presents the pin assignments.

High-speed writing

FRAM has an equivalent reading and writing period and is a nonvolatile memory that can be used in a similar manner to SRAM. As such, it is applied for a wide range of uses including as a substitute application for battery-backup SRAM. Since its writing period is short, the next reading or writing operation can be executed immediately after a writing operation, requiring no polling sequence for [ms] order as in Flash memory and EEPROM.

Photo 1 External View

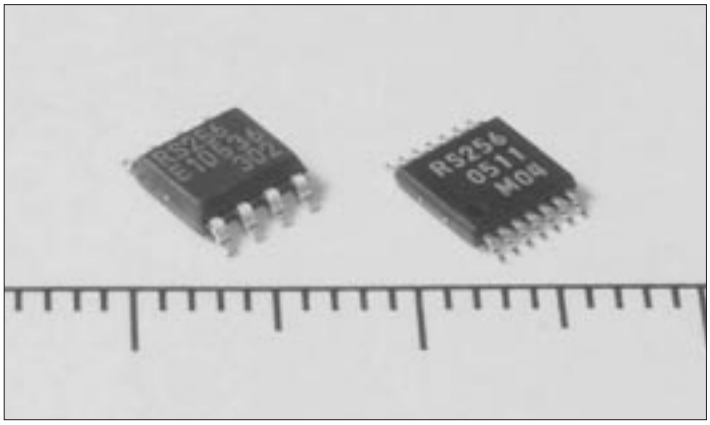
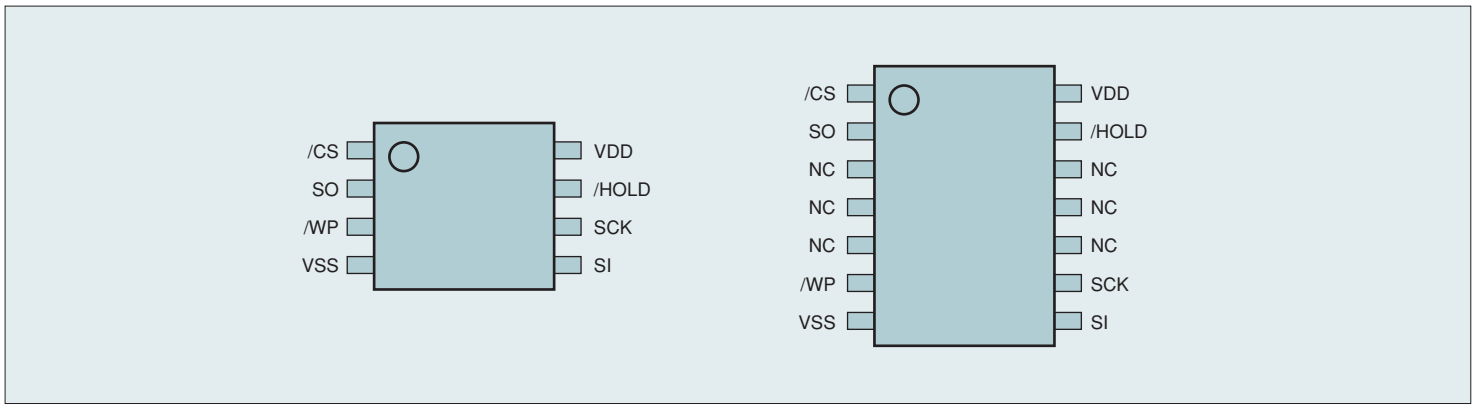


Figure 1 Pin Assignments



Furthermore, writing can be executed frequently without losing the next opportunity for writing because of polling.

This product, which is a serial interface FRAM, is capable of continuous reading and writing command execution just after a writing command. In addition, writing can be repeated with automatic incrementing of the address by one command. In this case, there is no restriction to the byte number for a single writing as in Flash memory or EEPROM page writing, and the entire memory cell can be written at once. Since there is no polling, the execution period is not extended even when a writing command is repeated with random access.

Energy saving

Since this product has a short writing period, the power required for a single writing (power consumption×writing period) is approximately 1/7000 that of the equivalent EEPROM product.

Fig.2 presents the power (=power consumption) per unit time for writing frequency.

This product enables extremely low power consumption in applications with low writing frequencies such as game machines, measuring devices, copy machines, and printers.

Fig.3 presents a block diagram.

Functions

Status register

Fig.4 presents the status register for this product. This product incorporates an 8-bit status register; bits 2 to 7 are nonvolatile memory.

- WPEN (Status Register Write Protect): WPEN protects the writing on the status register in connection with /WP input.
- BP1, BP0 (Block Protect): Defines the block size for writing protection in the WRITE command.
- WEL (Write Enable Latch): Indicates that the FRAM memory and status register can be written.
- Bit 0 is fixed to "0." Bits 4, 5, and 6 are not used.

Commands

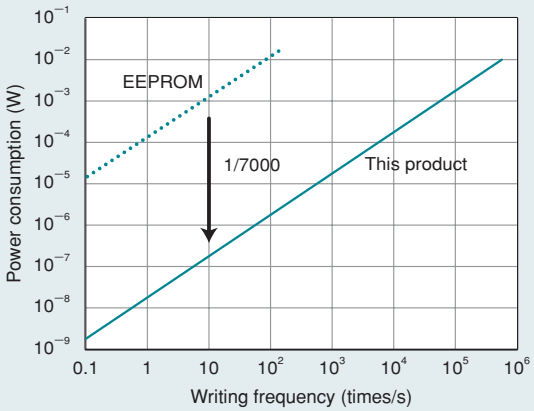
This product accepts six types of commands that are specified by operation code.

Table 1 lists the operation codes.

This product executes the serial input of operation code, address, and writing data. Reading data is also output serially.

- WREN: Sets WEL.
- WRDI: Resets WEL.

Figure 2 Power Consumption for Writing



- RDSR: Reads out the data in the status register.
- WRSR: Writes data into the nonvolatile memory bit of the status register.
- READ: Reads out the data in the FRAM memory cell array.

Fig.5 presents the READ sequence. Successive reading is realized by automatic incrementing of the address.

- WRITE: Writes data into the FRAM memory cell array.

Fig.6 presents the WRITE sequence. Successive writing is possible through automatic incrementing of the address.

Protection block

Depending on the values of BP1 and BP0 in the status register, a writing protection block for the WRITE command can be set up.

Table 2 presents the protection blocks.

Writing protection

Table 3 presents the writing protection available. As shown in the table, writing operations by the WRITE command and WRSR command are protected depending on the value of WEL, WPEN, and /WP.

Table 4 presents the AC characteristics, **Fig.7** the serial data timing, and **Fig.8** the roadmap of single-unit FRAM.

Future Development

The cumulative number of FRAM shipments from FUJITSU has already exceeded 200 million. We will continue to promote the density increase and speedup of FRAM and develop serial interface FRAMs as a leading manufacturer of FRAM products. ✱

Figure 4 Status Register

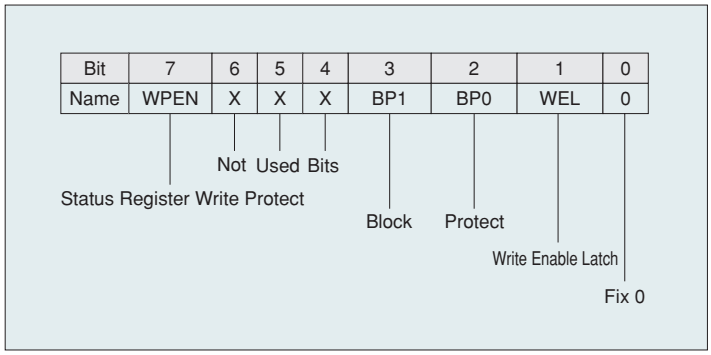


Table 1 Operation Codes

Command	Description	Op-code
WREN	Set Write Enable Latch	0000 0110b
WRDI	Reset Write Enable Latch	0000 0100b
RDSR	Read Status Register	0000 0101b
WRSR	Write Status Register	0000 0001b
READ	Read Memory Code	0000 0011b
WRITE	Write Memory Code	0000 0010b

Figure 3 Block Diagram

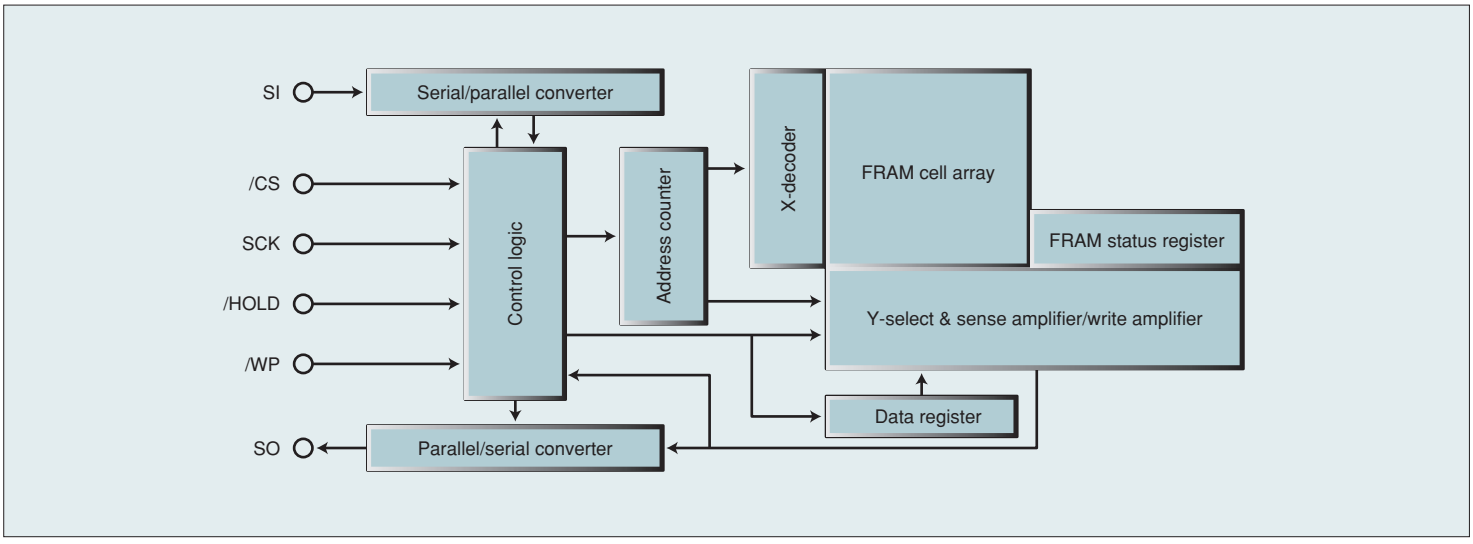


Figure 5 READ Sequence

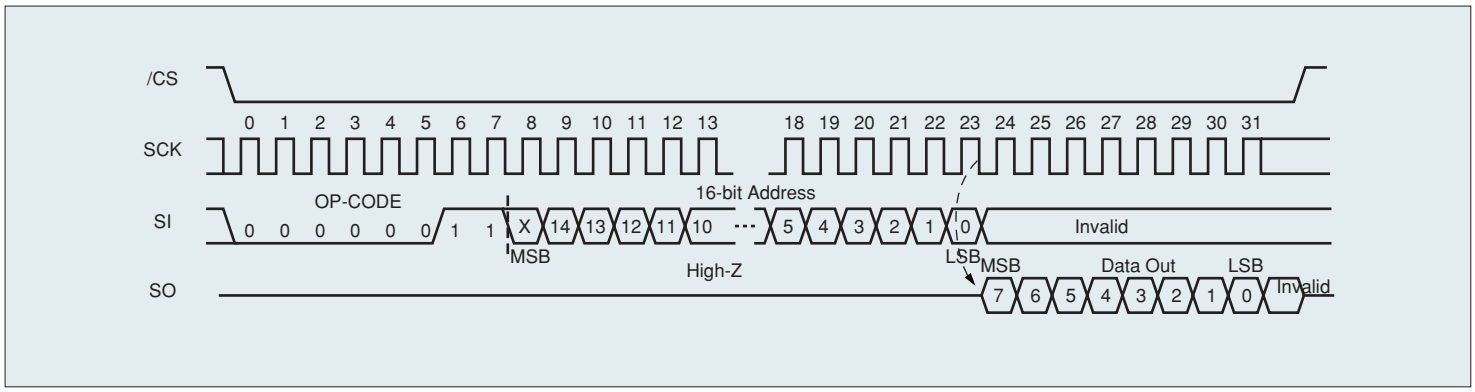


Figure 6 WRITE Sequence

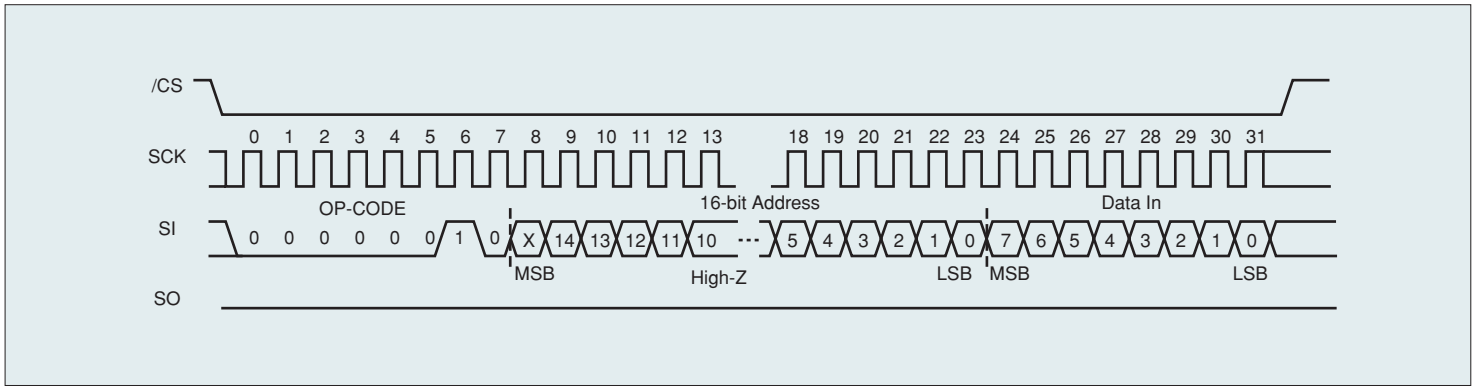


Table 2 Protection Blocks

BP1	BP0	Protected Block
0	0	None
0	1	6000h to 7FFFh (upper 1/4)
1	0	4000h to 7FFFh (upper 1/2)
1	1	0000h to 7FFFh (all)

Table 3 Writing Protection

WEL	WPE	/WP	Protected Blocks	Unprotected Blocks	Status Register
0	×	×	Protected	Protected	Protected
1	0	×	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Table 4 AC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
fCK	SCK Clock Frequency	0	——	15	MHz
tCH	Clock High Time	30	——	——	ns
tCL	Clock Low Time	30	——	——	ns
tCSU	Chip Select Setup Time	10	——	——	ns
tCSH	Chip Select Hold Time	10	——	——	ns
tOD	Output Disable Time	——	——	20	ns
tODV	Output Data Valid Time	——	——	35	ns
tOH	Output Hold Time	0	——	——	ns
tD	Deselect Time	60	——	——	ns
tR	Data In Rise Time	——	——	50	ns
tF	Data Fall Time	——	——	50	ns
tSU	Data Setup Time	5	——	——	ns
tH	Data Hold Time	5	——	——	ns
tHS	/HOLD Setup Time	10	——	——	ns
tHH	/HOLD Hold Time	10	——	——	ns
tHZ	/HOLD Low to High-Z	——	——	20	ns
tLZ	/HOLD High to Data Active	——	——	20	ns

Figure 7 Serial Data Timing

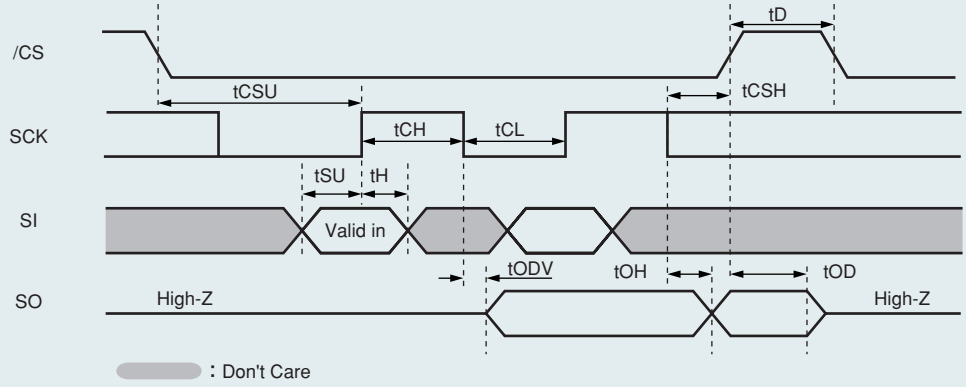


Figure 8 Roadmap of Single-Unit FRAM