R2A20178NP

8-bit 8ch Multiplying D/A Converter with Buffer Amplifiers

R03DS0021EJ0100
Rev.1.00
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Description

The R2A20178 is a CMOS 8-bit 8ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by simple three-wiring method (DI, CLK, LD), and it is suitable for a use in automatic adjustment applications in conjunction with a MCU. The reference voltage terminals (V_{DA}ref1, V_{DA}ref2) are 4ch x 2 configuration, and the 4 quadrant operation is possible.

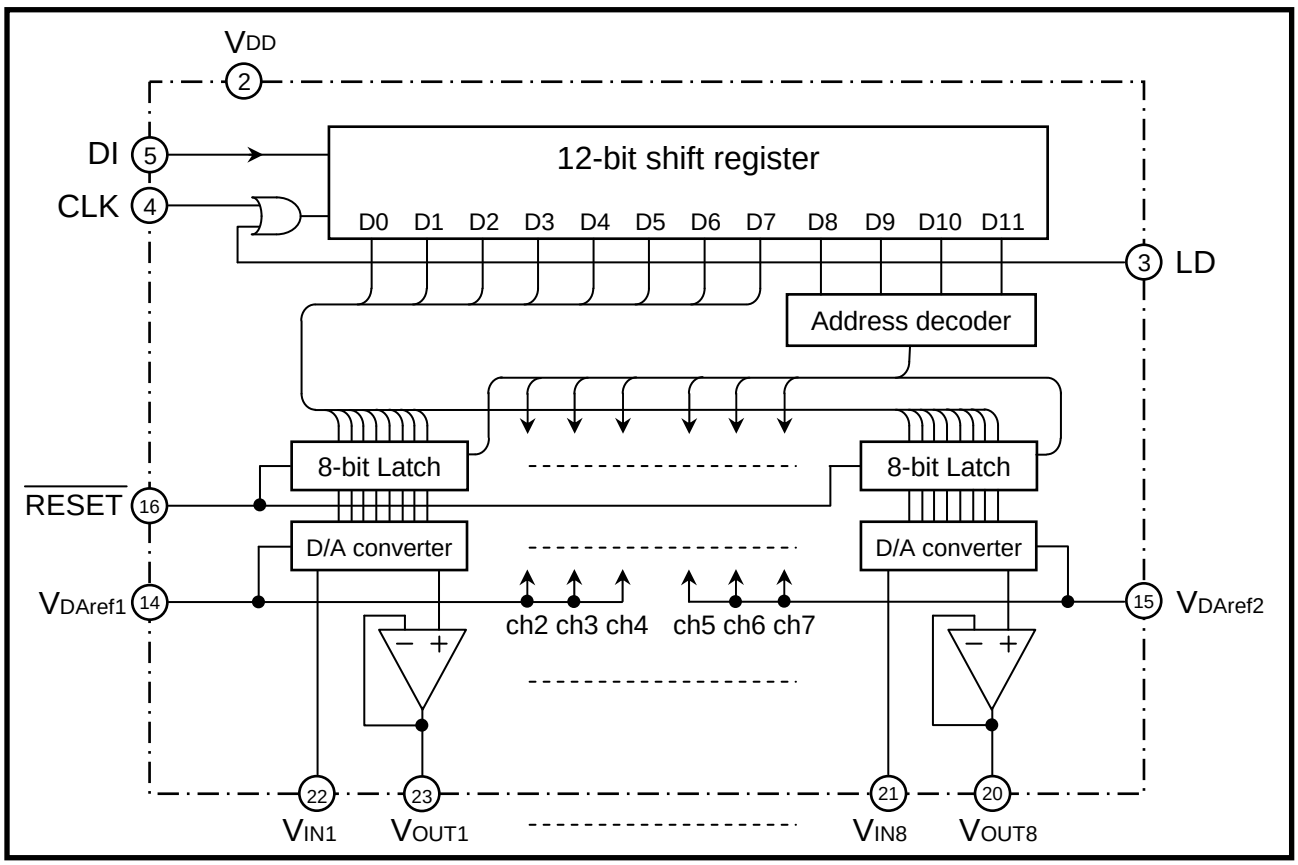
Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Three-wiring serial data transmission
- High performance 8ch D/A converter employing an R-2R with higher-order segment method
- 8 buffer amplifiers operating in a whole supply voltage range from V_{DD} to GND
- High anti-oscillation stability for capacitive loads
- 4 quadrant multiplication
- Very small package : QFN (pin pitch 0.5mm)

Application

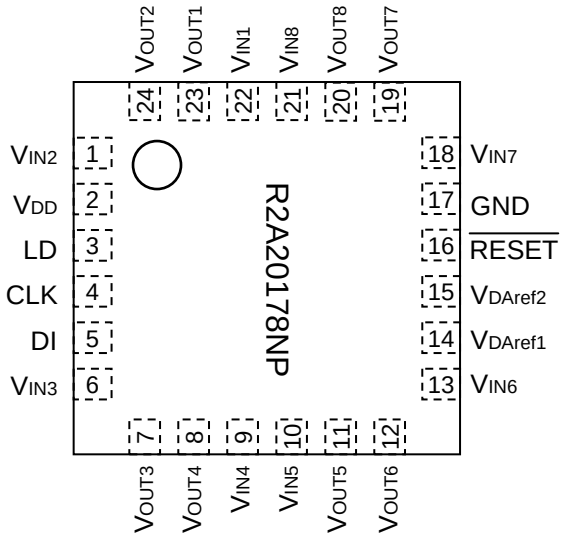
- Digital to analog conversion for consumer and industrial equipment.
- Self adjustment by combination with microcomputer and EEPROM (substitution of half fixed resistance)
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Voltage control of transmission power amplifier of transceiver

Block Diagram



Pin Arrangement

R2A20178NP (Top view)



Outline : PWQN0024KD-A [NP]

Pin Description

Pin No.	Pin Name	Function
3	LD	A low state of LD enables data of DI loading to the 12-bit resister. During a rising edge of LD, the data in the 12-bit shift register on a rising edge of register.
4	CLK	Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge Of the clock.
5	DI	Serial data input. The serial data length is 12-bit.
16	$\overline{\text{RESET}}$	Reset 8-bit latches. A low state of $\overline{\text{RESET}}$ clear the all 8-bit latches.
23	V_{OUT1}	D/A converter output with 8-bit resolution
24	V_{OUT2}	
7	V_{OUT3}	
8	V_{OUT4}	
11	V_{OUT5}	
12	V_{OUT6}	
19	V_{OUT7}	
20	V_{OUT8}	
2	VDD	Power supply
17	GND	Ground
22	V_{IN1}	D/A converter input
1	V_{IN2}	
6	V_{IN3}	
9	V_{IN4}	
10	V_{IN5}	
13	V_{IN6}	
18	V_{IN7}	
21	V_{IN8}	
14	V_{DAref1}	D/A converter reference voltage input (ch1 to ch4). $V_{OUT}= (V_{IN}-V_{DAref}) \times n/256+V_{DAref1}$
15	V_{DAref2}	D/A converter reference voltage input (ch5 to ch8). $V_{OUT}= (V_{IN}-V_{DAref}) \times n/256+V_{DAref2}$

Absolute Maximum Ratings

(Ta= +25deg unless otherwise noted)

Item	Symbol	Conditions	Ratings	Unit
Supply voltage (for digital)	V_{DD}		-0.3 to +6.5	V
Digital input voltage	V_{IND}		-0.3 to +6.5	V
Analog input voltage	V_{IN}		-0.3 to V_{DD}+0.3 <+6.5	V
Analog output voltage	V_{OUT}		-0.3 to V_{DD}+0.3 <+6.5	V
D/A reference voltage	V_{DAref}		-0.3 to V_{DD}+0.3 <+6.5	V
Power dissipation	Pd	Ta= +85deg	300	mW
Thermal derating	K theta	Ta> +25deg	7.5	mW/deg
Operating temperature	Topr		-30 to +85	deg
Storage temperature	Tstg		-40 to +125	deg

Electrical Characteristics

< Analog/Digital Common Part >

(V_{DD},V_{IN}= +5V +/-10%, V_{DD}>V_{IN}, GND=V_{DAref1}=V_{DAref2} = 0V, Ta = -30 to +85deg, unless otherwise noted.)

Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Supply voltage	V_{DD}		2.7	5.0	5.5	V
Supply current	I_{DD}	CLK =1MHz, V_{DD} =5V, I_{AO} =0µA	-	-	2.0	mA

< Digital Part > (V_{DD},V_{IN} = +5V +/-10%, V_{DD}>V_{IN}, GND=V_{DAref1}=V_{DAref2} = 0V, Ta = -30 to +85deg, unless otherwise noted.)

Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Input leak current	I_{ILK}	V_{IN} = 0 to V_{DD}	-10	-	10	µA
Digital input "Low" voltage	V_{IL}		-	-	0.2 V_{DD}	V
Digital input "High" voltage	V_{IH}		0.8 V_{DD}	-	-	V

< Analog Part > (V_{DD},V_{IN} = +5V +/-10%, V_{DD}>V_{IN}, GND=V_{DAref1}=V_{DAref2} = 0V, Ta = -30 to +85deg, unless otherwise noted.)

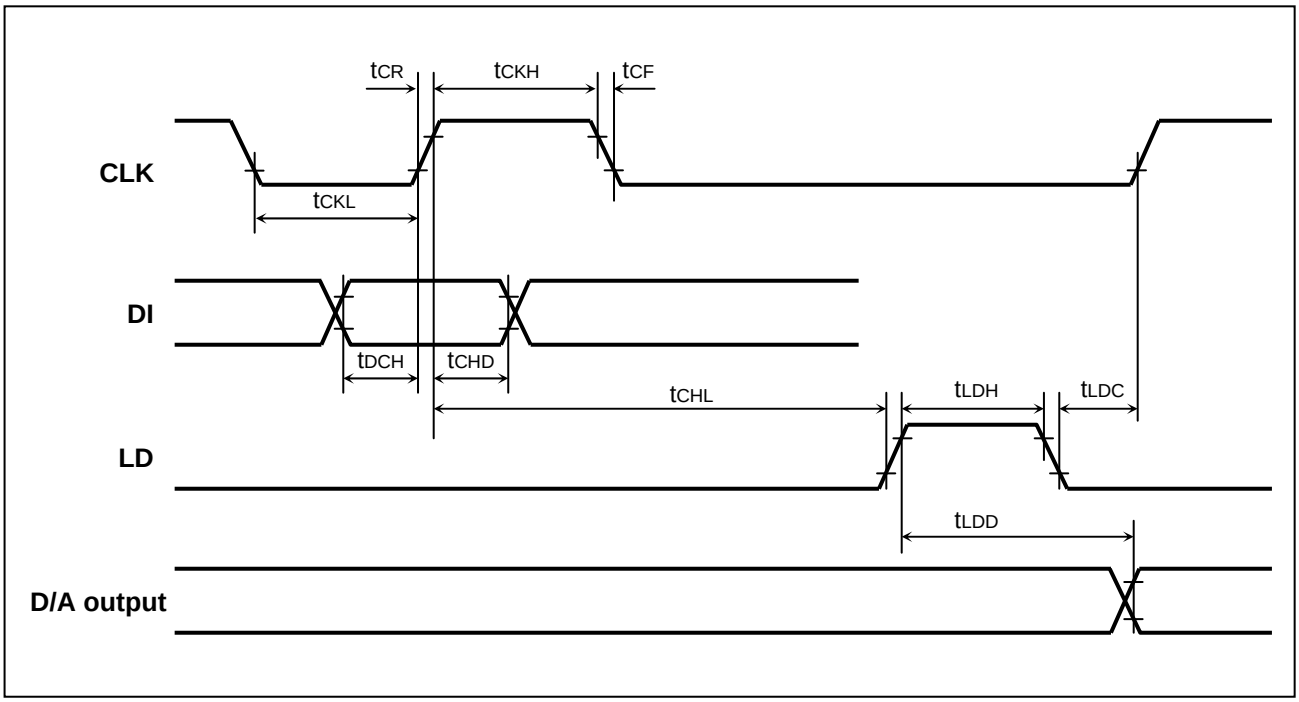
Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Input current	I_{IN}	V_{IN} =5V, V_{DAref} =0 V, Proportional to Max. input current condition (V_{IN} –V_{DAref}) and digital data of each channels	-	-	0.3	mA
D/A reference input current	I_{DAref}	V_{IN1} to V_{IN8} =5V, V_{DAref} =0 V, Proportional to Max. input current condition (V_{IN} –V_{DAref}) and digital data of each channels	-2.4	-	-	mA
Resolution	RES		-	8	-	bit
Differential nonlinearity	DNL	V_{DAref1} =V_{DAref2} =0.05V, Without load (I_{VOUT}= 0µA)	-0.7	-	0.7	LSB
nonlinearity	NL		-1	-	1	LSB
Buffer amplifier output voltage range	V_{AO}	I_{AO} = +/-100 µA	0.1	-	V_{CC} – 0.1	V
		I_{AO} = +/-500 µA	0.2	-	V_{CC} – 0.2	
Buffer amplifier output current range	I_{AO}	Upper saturation voltage =0.4V, Lower saturation voltage =0.4V	-1	-	1	mA
Output capacitive load	C_O		-	-	0.1	µF
Buffer amplifier output impedance	R_O		-	5	-	ohm

AC Characteristics

(V_{DD},V_{IN} = +5V +/-10%, V_{DD}>V_{IN}, GND=V_{DAref1}=V_{DAref2} = 0V, Ta = -30 to +85deg, unless otherwise noted.)

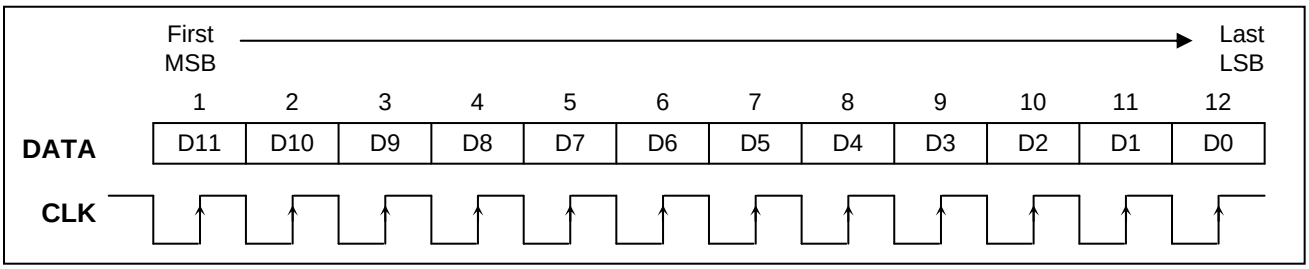
Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Clock “L” pulse width	t_{CKL}		200	-	-	ns
Clock “H” pulse width	t_{CKH}		200	-	-	ns
Clock rise time	t_{CR}		-	-	200	ns
Clock fall time	t_{CF}		-	-	200	ns
Data setup time	t_{DCH}		60	-	-	ns
Data hold time	t_{CHD}		100	-	-	ns
LD setup time	t_{CHL}		200	-	-	ns
LD hold time	t_{LDC}		100	-	-	ns
LD “H” pulse duration time	t_{LDH}		100	-	-	ns
D/A output settling time	t_{LDD}	C_L <100pF, V_{OUT} : 0.5←→4.5V, Time until the output becomes the final value of 1/2 LSB	-	-	300	µs
RESET “Low” level minimum pulse width	t_{RL}		200	-	-	ns

Timing Chart



Digital Data Format

12-bit serial data



Data Assignment

D8	D9	D10	D11

: DAC select data

D0	D1	D2	D3	D4	D5	D6	D7

: DAC data

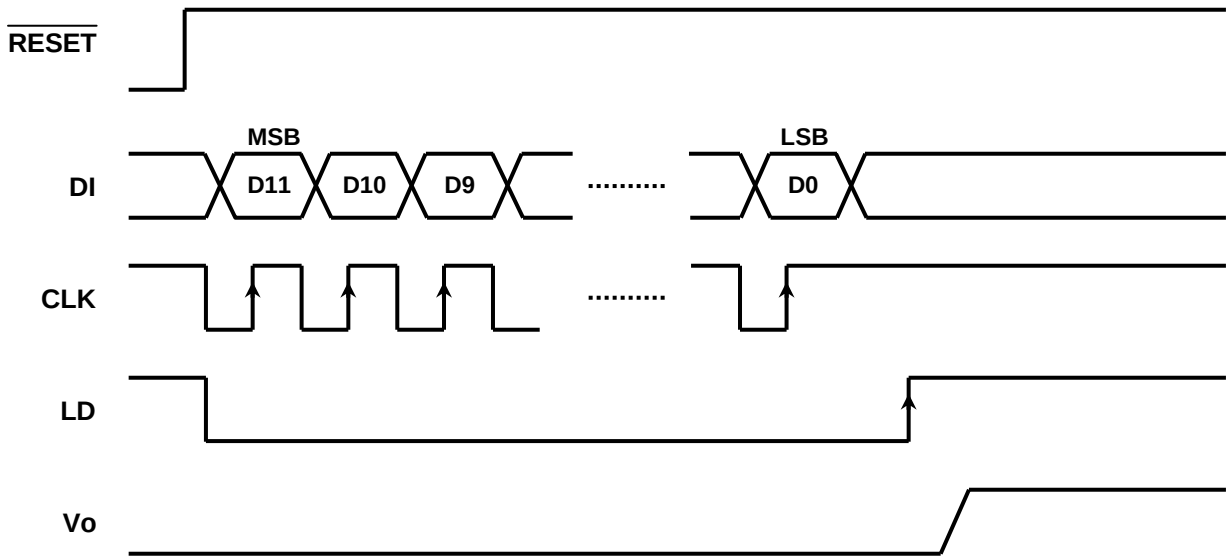
DAC select data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	V_{OUT1} selection
0	0	1	0	V_{OUT2} selection
0	0	1	1	V_{OUT3} selection
0	1	0	0	V_{OUT4} selection
0	1	0	1	V_{OUT5} selection
0	1	1	0	V_{OUT6} selection
0	1	1	1	V_{OUT7} selection
1	0	0	0	V_{OUT8} selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	DAC Output
0	0	0	0	0	0	0	0	V_{DAref}
1	0	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 1 + V_{DAref}$
0	1	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 2 + V_{DAref}$
1	1	0	0	0	0	0	0	$(V_{IN} - V_{DAref}) / 256 \times 3 + V_{DAref}$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	$(V_{IN} - V_{DAref}) / 256 \times 255 + V_{DAref}$

Timing Chart (Model)



Note: Input data is carried out LD signal low besides CLK signal positive edge.
CLK, LD is kept generally high level.

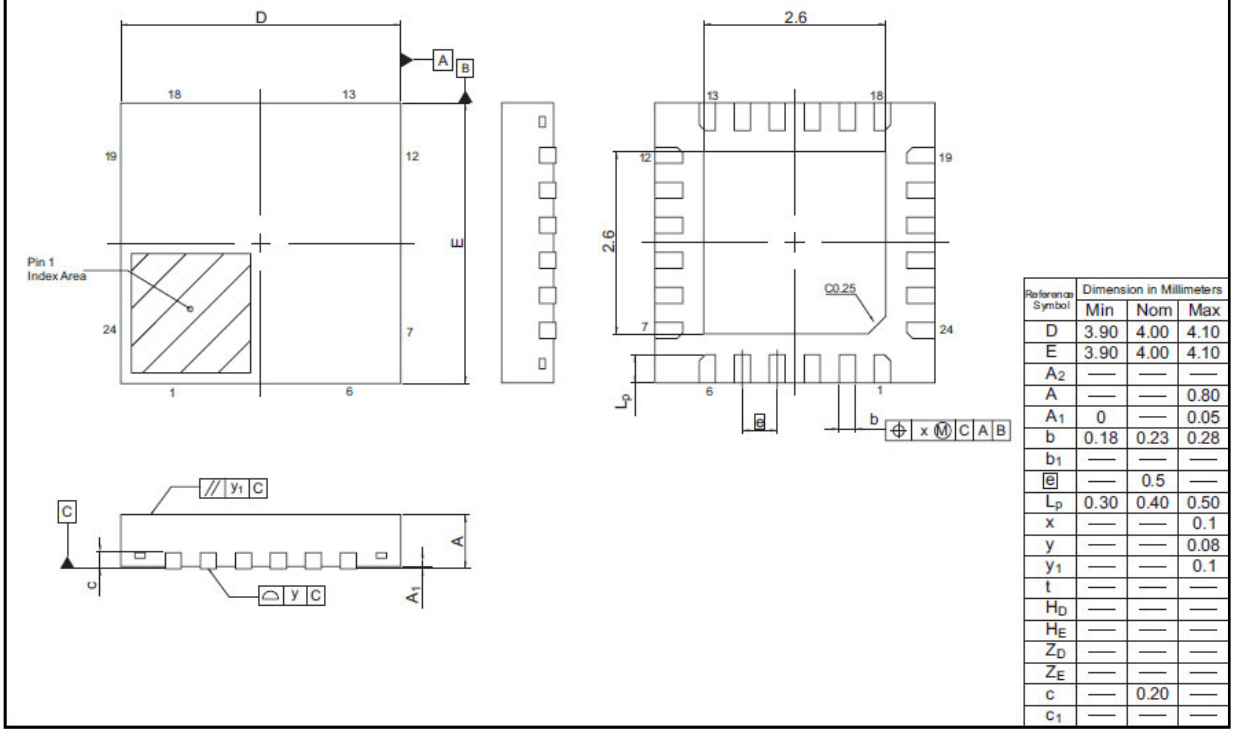
Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20178NP	QFN-24	PWQN0024KD-A	NP	Embossed Taping/2,500 pcs.

Package Dimensions

PWQN0024KD-A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN24-4x4-0.50	PWQN0024KD-A	—	0.037g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.90	4.00	4.10
E	3.90	4.00	4.10
A_2	—	—	—
A	—	—	0.80
A_1	0	—	0.05
b	0.18	0.23	0.28
b_1	—	—	—
e	—	0.5	—
L_p	0.30	0.40	0.50
x	—	—	0.1
y	—	—	0.08
y_1	—	—	0.1
t	—	—	—
H_D	—	—	—
H_E	—	—	—
Z_D	—	—	—
Z_E	—	—	—
c	—	0.20	—
c_1	—	—	—

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